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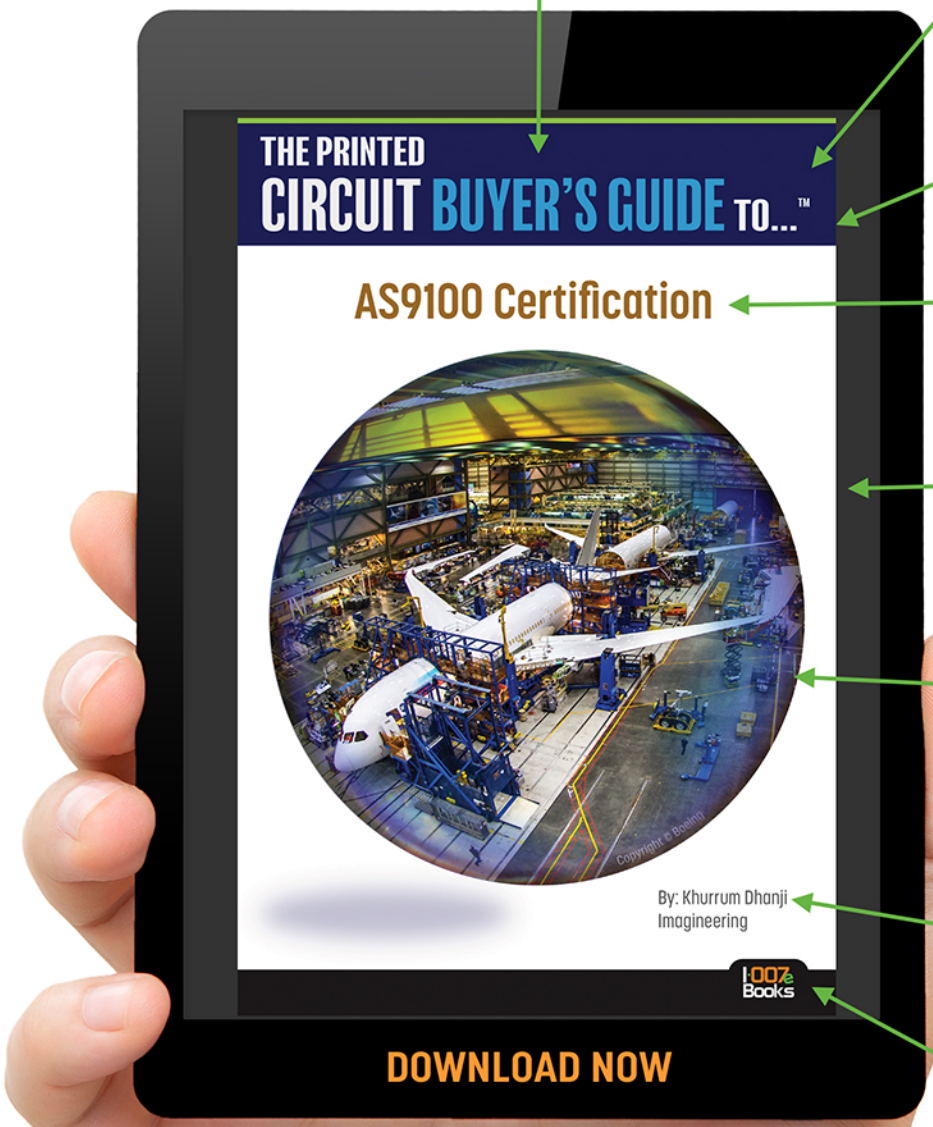

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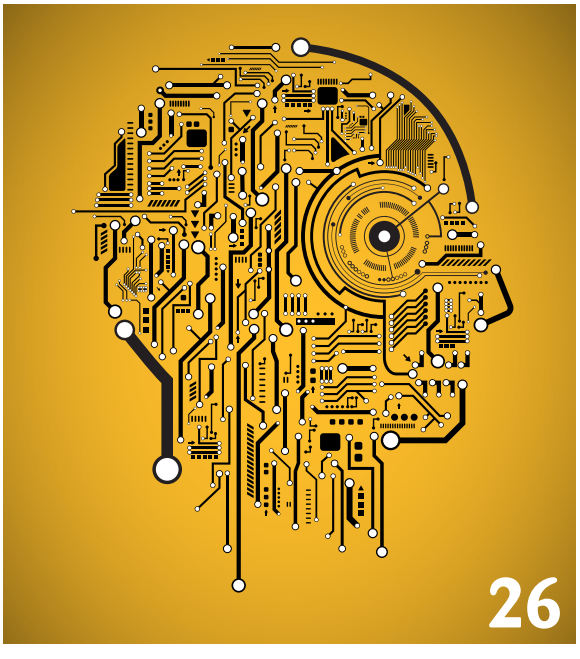

The DFM Issue

PCB designers have been focusing on good DFM practices for decades now. But many fabricators still see many of the same old design mistakes and miscues, not to mention a few new ones. What's going on? In this issue, designer and CID instructor Kelly Dack explains why solid DFM techniques sometimes require designers to take back control from their increasingly automated EDA tools. Next, in an interview, Gary Ferrari of FTG Corp. discusses the art and science of DFM techniques, as well as some common problems that designers could easily avoid. We've also included a handy index of recent DFM articles.

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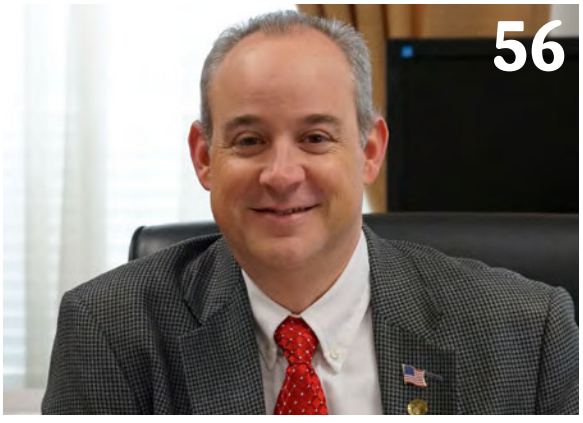

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True DFM: We're Not There Yet

by Andy Shaughnessy
I-CONNECT007

When I first started covering PCB design, it didn't take long for me to realize that I had a lot to learn. In addition to learning all I could about PCB design, fabrication, assembly, and the many technical and international challenges facing the industry, I needed to get up to speed, and pronto, on dozens of abbreviations.

I'd been down the abbreviation road before as a newspaper reporter. I used to believe that no one could top law enforcement's incessant use of abbreviations. But the PCB industry outabbreviates the police, hands down. It's not even a close contest.

Besides the usual suspects such as PCB, EDA, CAM and CAD (the last two are also acronyms, incidentally, since they spell pronounceable words), I was faced with HATS, HASL, QFP, PQFP, SMOGB, and LCCC, just to name a few. You know all of these…you have to in order to do your job.

Then there were all of the "design fors," like DFM, DFA, DFT, DFE, and DFX. I have to admit, DFM seemed a little bit superfluous at first. Wouldn't every board you design be designed for manufacturing?

So began my introduction to DFM. The PCB industry isn't the only one to embrace DFM; tooling, sheet metal stamping and fabrication, and a variety of other manufacturing segments have adopted DFM guidelines for exactly the same reason: Their designers were creating products that were difficult and/or expensive to manufacture, often using custom parts when commercial off-the-shelf parts would suffice.

Interesting fact: According to some estimates, up to 70% of an end-product's manufac-

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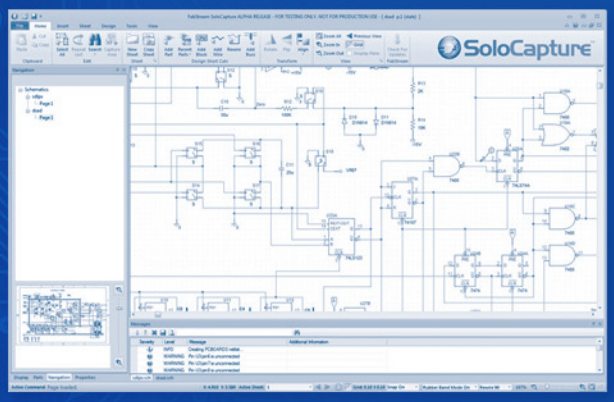

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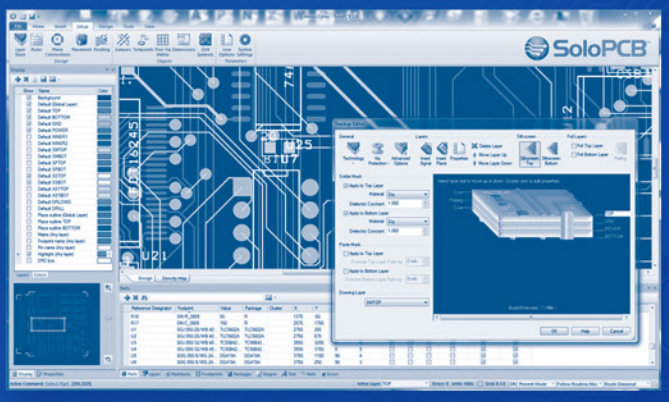

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turing costs are determined during the design stage.

A lot of PCB designers tell me they haven't visited a fabricator in years, and some have never been inside a manufacturing facility. Does the same hold true for designers of sheet metal and tooling?

The push for DFM in the PCB world was in full swing by the 1990s. Designers swore they would never "throw the PCB design over the wall" again, so great was their devotion to solid DFM practices. DFM classes at industry conferences began filling up as designers tried to learn all they could about fabrication processes. Designers began communicating with their fabricators from the beginning of the design process.

By all accounts, the situation has greatly improved. Thanks, in part, to DFM techniques, many designs are now "right the first time." But fabricators are still receiving bad or incomplete data, especially from new customers. And some designs are still expensively over-constrained, leading to the dreaded phone calls to the designer at 4:45 pm on a Friday.

This month, we focus on DFM, starting with our feature story by PCB designer and CID instructor Kelly Dack. He explains how today's advanced EDA tools have to be tightly controlled to achieve good DFM practices, even for issues as simple as copper-to-edge spacing, and why designers should check with IPC-2221 in such instances. In an interview, Gary Ferrari of FTG Corp. discusses the art and science of DFM techniques, and some of the most prevalent, yet easily avoidable design process and data errors that fabricators encounter. We've also provided an index of the Top 10 recent DFM articles published by I-Connect007 over the past few years. Some of these useful articles have garnered thousands of views. We also have an interview with Altium's Rainer Asfalg, who explains what it means to be a designer, and why great EDA tools use automation to help designers deal with manufacturing data.

We also have an article by Lance Olive of Better Boards Inc., a design bureau based in Cary, North Carolina. Lance discusses the many challenges related to selling EDA services in the 21st century, and how design service providers can best differentiate themselves. And columnist Barry Olney details the proper placement of decoupling capacitors that are necessary to complement the power distribution network.

I hope you all had plenty of rest over the holiday, because it looks like it's going to be a busy 2017. We'll be bringing you coverage of DesignCon, IPC APEX EXPO, and the CPCA Show in Shanghai, China. If you can't make it to these trade shows, don't worry; we've got you covered.

Have a happy new year! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 17 years. He can be reached by clicking here.

New Hybrid Material for Spin Transistors of the Future

Spin-based transistors could replace conventional transistors in the future. Spin transistors require significantly less energy, but industrial conversion has so far failed due to the lack of a suitable material. A young scientist, Zeila Zanolli, has found a novel combination of graphite and barium manganese oxide, which meets the contradictory requirements. The hybrid material allows both precise spin alignment and good spin transport, as demonstrated by simulations on supercomputers at the Jülich Supercomputing Center (JSC).

Transistors are probably the most important basic building blocks of modern memory sticks and processors. The switching processes in a spin-based transistor, on the other hand, are based on changes in the electron spin, like all applications in the field of spintronics.

However, the implementation of spin transistors is made more difficult by contrasting material requirements. Traditional semiconductors, such as those currently used in chip manufacturing, offer a strong spin-orbit coupling: the electron spin can be aligned well with an external field.

A Handy Compilation of Our Top 10 DFM Articles

by Andy Shaughnessy
I-CONNECT007

When we started working on this issue, I searched through our files and found that we've published some great DFM articles over the past year or so. While topics like signal integrity tend to get most of the limelight, in the end it all comes down to solid DFM practices. So, without further ado, we present this compilation of our Top 10 DFM articles and columns, culled from the pages of *The PCB Design Magazine* and *The PCB Magazine*. Enjoy.

①

The Top 10 Ways Designers Can Increase Profits

So, can you truly increase profitability through PCB design practices? Yes, you can. And it starts with a philosophy that embraces DFM techniques. Then you must be ready for the initial release to a fabricator by ensuring that you are communicating all of your specifications and needs clearly to the fabrication house so that you get an accurate quote. By Mark Thompson.

②

Beyond Design: The Need for Speed—Strategies for Design Efficiency

Years of experience with one EDA tool obviously develops efficiency, whether the tool be high-end feature-packed or basic entry-level. However, there comes a time, with the fast development pace of technology, that one should really consider a change for the better to incorporate the latest methodologies. This month, I will look at productivity issues that impede the PCB design process. By Barry Olney.

③

Brooks' Bits: How Many Vias Does It Take To…?

Sounds like the opening words of a bad joke. Well, here's the answer, and it's no joke: One! That's right. No matter how much current you are putting down the trace, all you need is a single via. And a small one, at that. OK, that last statement might not be true in every single case. But it is true in a LOT more cases than you think. I will explain why in this column. By Douglas G. Brooks.

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4

Mark Thompson: It's All about Communication

During DesignCon, we talked with columnist Mark Thompson about why communication is paramount when designing and prototyping boards. Thompson also explained how designers can avoid making common mistakes that can set back an entire project. By Barry Matties and Andy Shaughnessy.

5

Trouble in Your Tank: Building Reliability into the PCB, Part 2

Many engineers have been in this situation: Process audits are completed. Personnel who have direct influence are properly trained. Analytical controls are in place. Great! Yet there are boards that are not meeting specification (IPC 6010 Series, IPC 600, IPC 610). And now the team has to deal with the rejects and provide corrective actions. By Michael Carano.

6

Against the Density Wall: Landless Vias Might be the Answer

I saw my first landless via multilayer while visiting NEC at Toyama, Japan in 1985. They were an enormous automated facility making Japanese telecom and mainframe computer boards, kind of like IBM and Western Electric rolled into one. NEC was using the liquid electrophoretic, positive-acting photoresist process with panel-plating. I wouldn't see another landless via multilayer until our Japanese partner, OKI, introduced it to us in 1988. By Happy Holden.

7

From the CAM Shop: Tight Tolerance Design Tips

After you finish your design, it winds up in the hands of people like Mark Thompson, the man who runs the CAM department at Prototron Circuits in Redmond, Washington. For this issue, we asked Mark to discuss the today's tight tolerances, some of the problems they can cause PCB designers, and what designers can do when dealing with shrinking features. By Andy Shaughnessy.

8

Designers Notebook: Flex and Rigid-Flex Circuit Design Principles, Part 1

Flex circuits have an advantage over hardwire interface because they fit only one way, eliminating wire routing errors as well as the time needed for testing and inspection. Furthermore, flex circuit conductor patterns will maintain uniform electrical characteristics, controlling noise, crosstalk, and impedance. By Vern Solberg.

9

Innovative Use of Vias for Density Improvements

The classic way to increase density is to reduce the trace and spacing. But in many high-speed board applications, the copper and dielectric losses from smaller traces, or the increased crosstalk from reduced spacings, do not permit this. Four old ideas used in board design and fabrication can offer some insight into how routing density can be increased. By Happy Holden.

10

Designing With Tighter Tolerances

David Ledger-Thomas is a PCB design engineer with Honeywell Aerospace. He's spent decades designing PCBs for a variety of applications, including defense, aerospace, computers, and high-performance audio. I asked David to share some of his thoughts on designing high-tech boards with increasingly finer spaces, traces and pitch. By Andy Shaughnessy. **PCBDESIGN**

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TRUE DFM:
Taking Control of Your EDA Tool

by Kelly Dack, CID+, CIT

We PCB designers are doing some truly great things with our layout tools. But we must remember that these tools are so powerful that they will sometimes allow us to design things that can't be manufactured! We must collaborate with our fabricator and assembly brethren and embrace the best DFM practices, or face the consequences downstream.

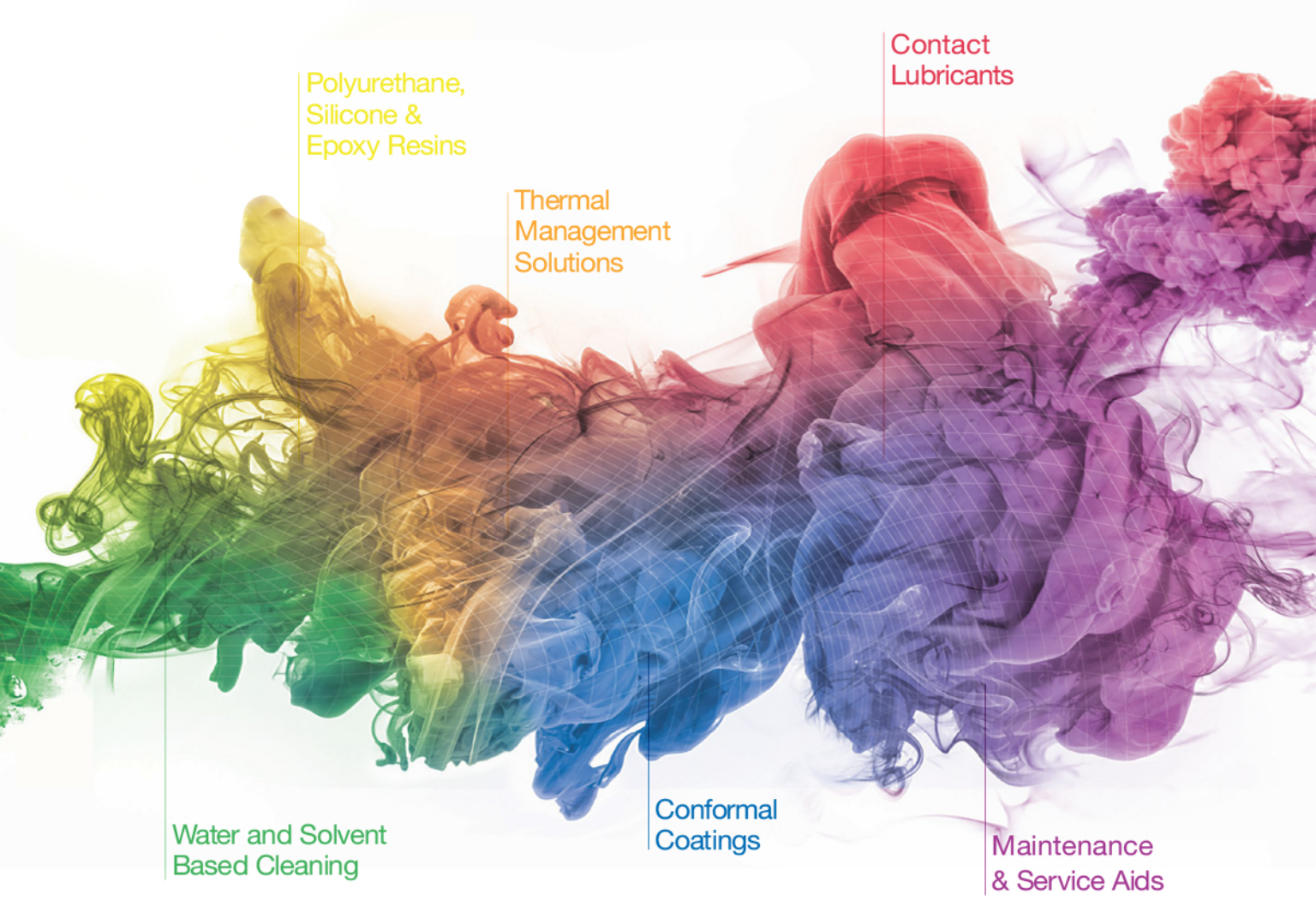
Something as seemingly simple as copper-to-edge spacing provides us with plenty of examples of DFM techniques, potentially good and bad.

Providing a sufficient amount of copper-to-edge spacing allows for the least costly manufacturing processes at the PCB fabrication and assembly levels. Extremely tight manufacturing etching and routing tolerances enable the close registration of copper to the cut board edge. On very tight layouts, we see a router profile that is intended to come within .007" of a copper trace. You may have seen closer—and even cases where the copper is designed to extend beyond the the board edge effectively wrapping around the board edge.

Granted, sometimes we designers intend for the copper to exist in close proximity to a board edge profile. When close copper-to-edge distance is intended, we ought to always be sure that the copper will end up protected with a coating of resin (if still laminated within the PCB) or plated with a surface finish in order to prevent oxidation or other forms of contamination.

While copper print and etch factors are more accurate than ever, and your PCB layout tool will allow you place that copper trace very close to that board edge, stop and wait a minute. Think about how this PCB will be fabricated and assembled.

If you don't know, set up a meeting with your PCB fabricator and assembler. Ask your manufacturing representatives about their capabilities and processes. Take note, though, with regard to the context of this conversation. If you ask how close you can design copper to the board edge, you will (and should) get an



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entirely different response than if you were to ask how far away should you keep your copper from the board edge. Here's why:

A PCB board fabricator is in the business of creating very fine images out of copper that will be matched with a drill pattern and registered very accuratly onto a board outline. If this is accomplished as a one-up PCB intended for manual assembly, there are few problems if the PCB is designed such that the copper-to-edge spacing comes within .010" (0.25 mm) or greater. But this scenario can plant the seed of failure if the board design is destined for automated assembly.

After a prototype PCB layout is blessed by the engineering team, the determination is made to get on with production. This is when the lightning bolt of manufacturing reality is set to strike. While the PCB fabricator has done his best to accurately route the board edge very close to the copper conductors as designed, this awsome capability has tied the hands of the assembly provider who may be under contract to build thousands of these PCBs. You see, a prototype fabricator's working panel can cut very close to the copper when building one-ups that will be shipped as single PCBs. But a PCB going to volume production must be designed to be included into an assembly array. There will be extra features which the assembly provider's engineers will be adding to allow for ease of depaneling or excising the boards from the array. These features all require varying amounts of space relative to the PCB edge.

Incorporating good DFM processes into a PCB means that the designer needs to have a familiarity of the processes that will remain available to the assembly provider after the PCB moves into production. One of the first things the assembly provider will be looking at is bare PCB material cost, and that means panel yield.

How many PCB images can fit onto a panel array? The assembly supplier's manufacturing engineers look very closely at the the PCB's shape and thickness. Additionally, copper-to-edge spacing is measured in order to derive the most robust, stable and easy to excise PCB retention solution satisfying the many various assembly and even test process.

The method of retention selected for the assembly array is based on quite a few factors, including:

- Whether the board edge is straight or curved
- The finished thickness of the PCB panel
- The dimensional tolerance requirements of the PCB edge
- Whether the PCB edge can tolerate a bare, frayed edge or must be smooth, sealed or plated

If there is insufficient copper-to-edge spacing for a viable panel excising method, the assembly engineer may be faced with a stop order until the proper permissions are obtained to direct the fabricator to modify the copper-to-edge spacing to allow for a particular excising method. It can take hours or days to obtain permission for this type of modification and is understadably awkward for all stakeholders in the manufacturing stream. The data for the modification is not included in Gerber and is usually added on a sub-set of fabrication documentation with a note and accompanying detail.

It is hoped that the our designer audience

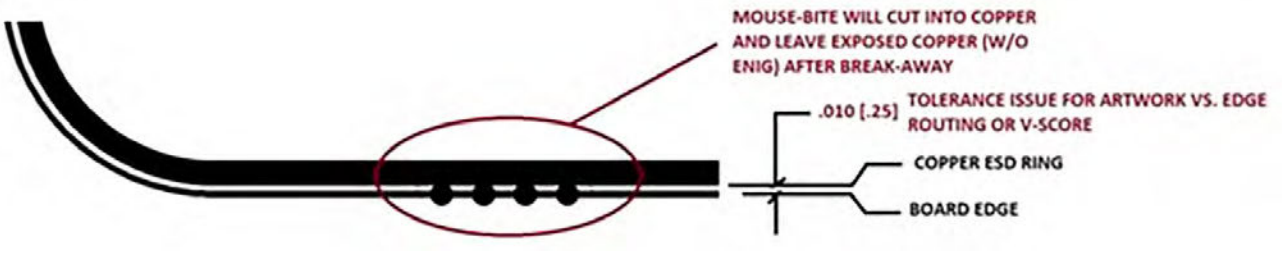

Figure 1: Example of insufficient copper-to-edge clearance.

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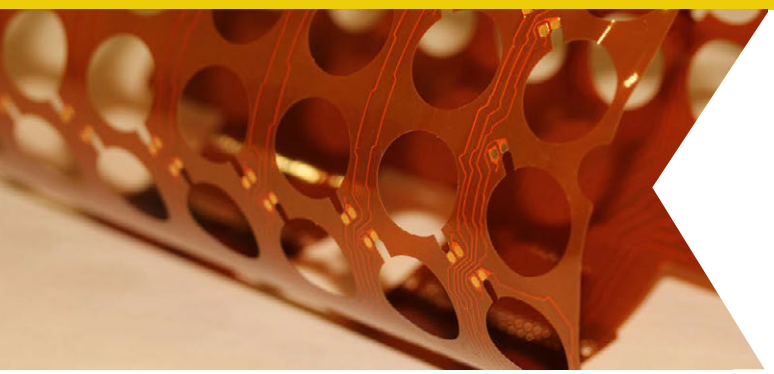

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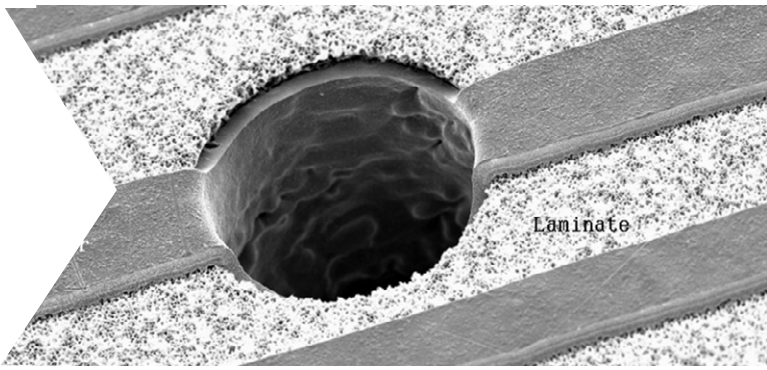

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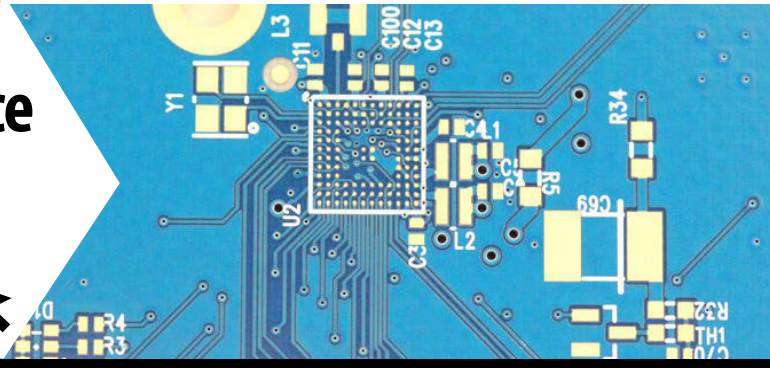

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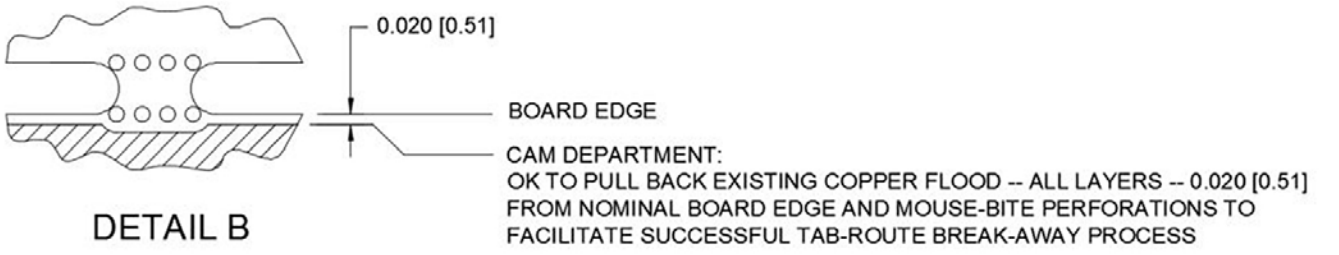

Figure 2: Fab note allowing CAM department to modify copper-to-edge spacing.

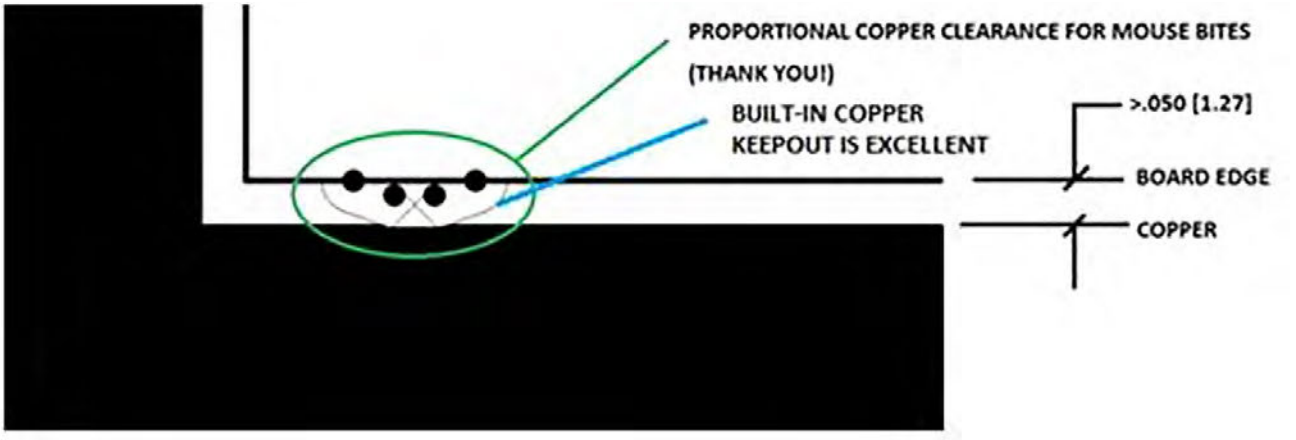

Figure 3: Example of robust copper-to-edge clearance on a low-density design.

knows that their design—their output data—serves as the hub of all of the manufacturing processes. It is so very important that insufficient or vague or unmanufacturable design data never be tossed over the wall to other stakholders. Providing insufficient copper-to-edge spacing is like a missing spoke on a racing bicycle's wheel. It needs to be addressed before the race begins. If addressed during the race, the rider may stop suddenly, surely affecting the other riders behind him.

But how does a designer know what copper-to-edge spacing value is adequate for keeping the bare copper stable and protected? An outdated rule of thumb back in the day was .050", but times have changed and manufacturing capabilities have too. Packaging densities have increased wildly and board real estate has never been more valuable.

So, if asked by someone in your design team how close the copper can get to the edge, what is a proper response? Hopefully, you can pull a copy of IPC-2221 off your shelf and turn right to section 10.1.1. Here you will see an industry standard recommendation which takes into account not only industry standard panel processing, but electrical clearances as well, as shown in Figure 4.

10.1.1 Edge Spacing Except for edge-board contacts, the minimum distance between conductive surfaces and the edge of the finished board, or a non-plated through hole, **shall** not be less than the minimum spacing specified in Table 6-1 of IPC-2221 plus 0.4 mm. Printed boards that slide into guides **shall** have a minimum external conductor to guide distance of 1.25 mm or minimum electrical clearance (see Table 6-1 of IPC-2221), whichever is greater. Special design applications in areas such as high voltage, surface mount, and radio frequency (RF) technology may require variances to these requirements. Ground and heat sink planes may extend to the edge when required by design.

Figure 4: Recommendation found in IPC-2221, section 10.1.1.

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6.3.1 B1-Internal Conductors Internal conductor-to-conductor, and conductor-to-PTH electrical clearance requirements at any elevation (see Table 6-1).

6.3.2 B2-External Conductors, Uncoated, Sea Level to 3050 m [10,007 feet] Electrical clearance requirements for uncoated external conductors are significantly greater than for conductors that will be protected from external contaminants with conformal coating. If the assembled end product is not intended to be conformally coated, the bare printed board conductor spacing **shall** require the spacing specified in this category for applications from sea level to an elevation of 3050 m [10,007 feet] (see Table 6-1).

6.3.3 B3-External Conductors, Uncoated, Over 3050 m [10,007 feet] External conductors on uncoated bare printed board applications over 3050 m [10,007 feet] require even greater electrical spacings than those identified in category B2 (see Table 6-1).

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Printed Board				Assembly		
	B1[1]	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.002 in]	0.1 mm [0.004 in]	0.1 mm [0.004 in]	0.05 mm [0.002 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.002 in]	0.1 mm [0.004 in]	0.1 mm [0.004 in]	0.05 mm [0.002 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]

Figure 5: The relevant portion of IPC-2221 (Table 6-1) of IPC-2221.

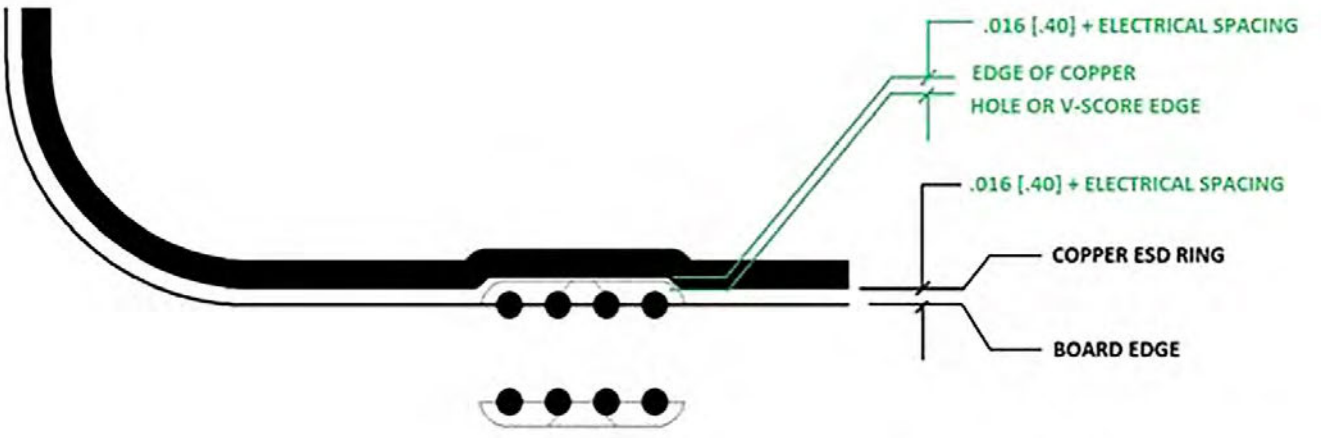

Figure 6: Recommendations for minimum copper-to-edge clearance.

So first start with the IPC-2221 recommendation of .4mm and then add an additional distance determined by Table 6-1 of IPC-2221 as shown in Figure 5. Keep in mind that the distance is expressed as a minimum. An example is shown in Figure 6.

Figure 7 shows an example of a mostly finished PCB. One of the last machining operations is routing or scoring, often per the assembly contract manufacturer's specification. Notice the PCB profile is curved. Will there be enough room for tab route?

In this case, it was determined that there was only enough room for tab. The mouse bite perforations were omitted due to the close proximity of traces. Will this cause another complication in the excising process? Perhaps a routing sub-operation? Snipping? Laser cutting?

A V-score scenario geometrically showing copper pull-back requirement at worst-case least/max material conditions. Note: The additional IPC-2221 electrical spacing is not included in Figure 9.

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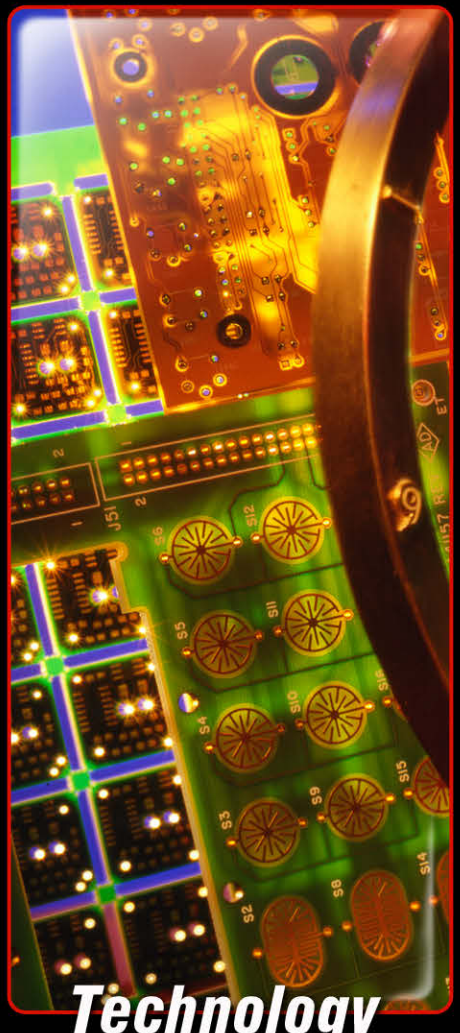
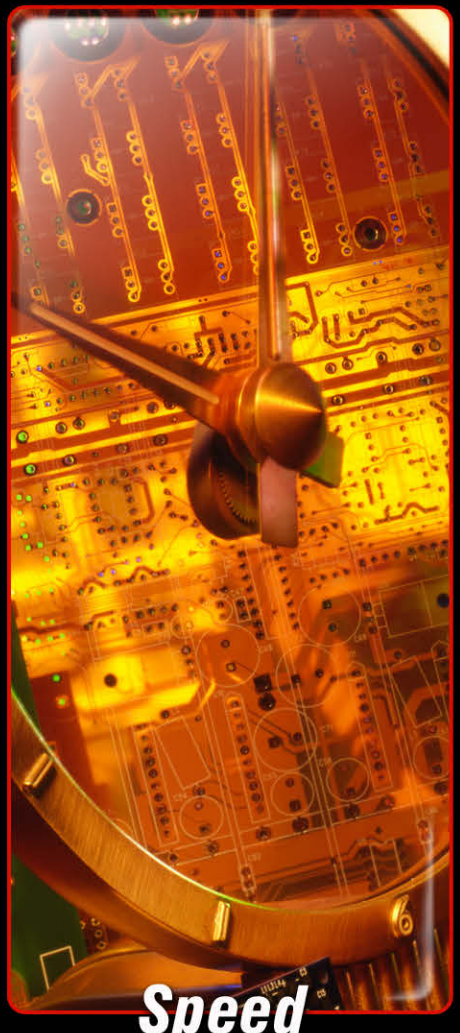
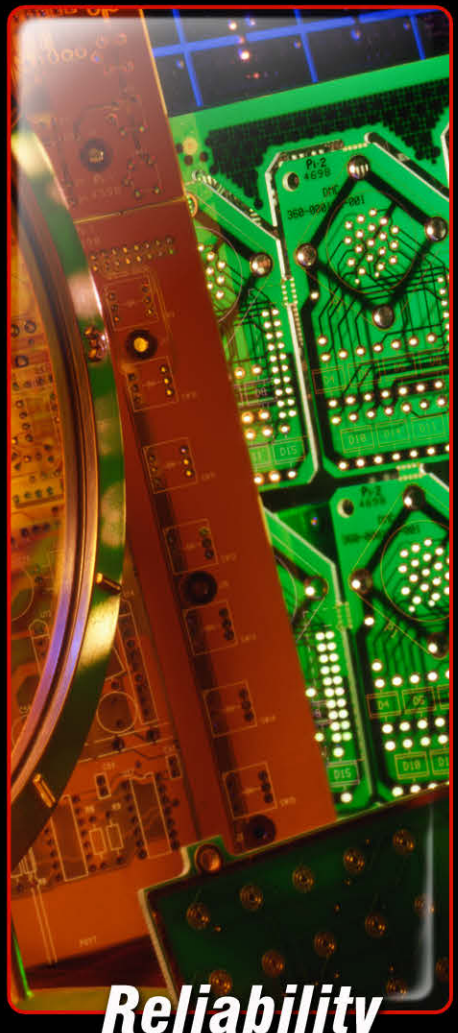


Technology



Speed



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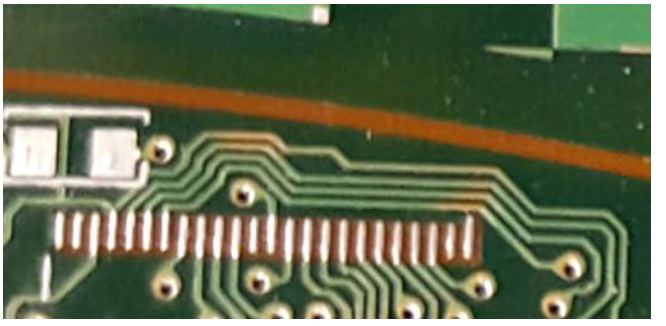


Figure 7: A nearly complete PCB, prior to routing.

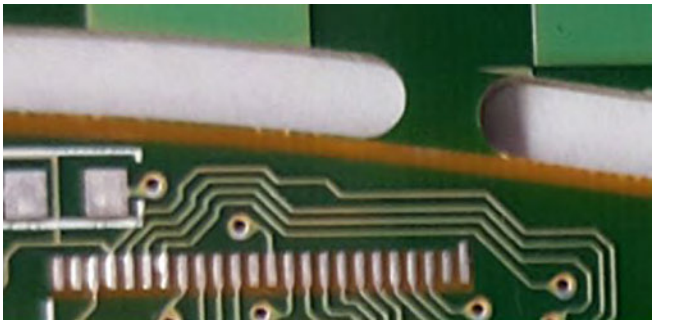


Figure 8: Example of board with tab only due to close proximity of traces.

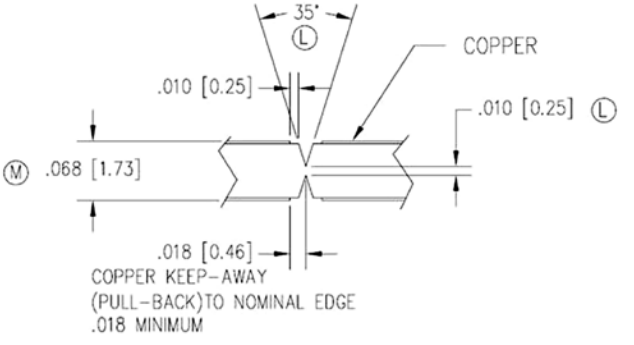


Figure 9: V-score scenario showing copper pull-back requirement at worst-case least/max material conditions.

IPC's organization has done a fine job of bringing together manufacturing representatives from all over the world to discuss, define and document standards for the design and manufacturing segments of our industry.

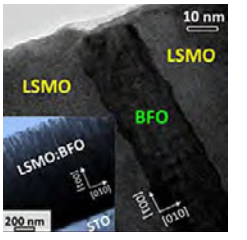
Yes, we in PCB design can perform some amazing things with today's layout tools. But we must remember not to get carried away. We must always check our settings. Remember, rarely do these settings show up as defaults in our software tools.

No matter how powerful our EDA tools are, we must still make that handshake with our fellow stakeholders—our fabrication and assembly providers. **PCBDESIGN**

Kelly Dack, CID+, CIT, provides design and manufacturing engineering services for an EMS provider in the Inland Pacific Northwest. He is also a CID instructor for EPTAC Corp. Kelly is a frequent contributor to *The PCB Design Magazine* and on-camera talent with the I-Connect007 Real Time video program. He may be reached at kelly@eptac.com.

Lining Up for New High-Density Memory Devices

To reduce the size and increase the durability of computers, cell phones, and other data-storing devices, scientists designed a structure made of tiny layers, which resembles a thick chessboard butcher-block table.



Scientists grew a vertically aligned nanocomposites lattice matched on a SrTiO3 (STO) substrate using laser deposition. By controlling the composition of the layers in the nanocomposites, scientists can tune the degree of magnetic exchange bias coupling strength. The research team conducted a microstructural analysis of the nanocomposite films using transmission electron microscopy and scanning transmission electron microscopy.

This new nanoscale architecture can be used for data storage in high-density memory devices as an alternative to conventional, in-plane magnetic exchange bias; such devices could provide more efficient performance.

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—David Dibble

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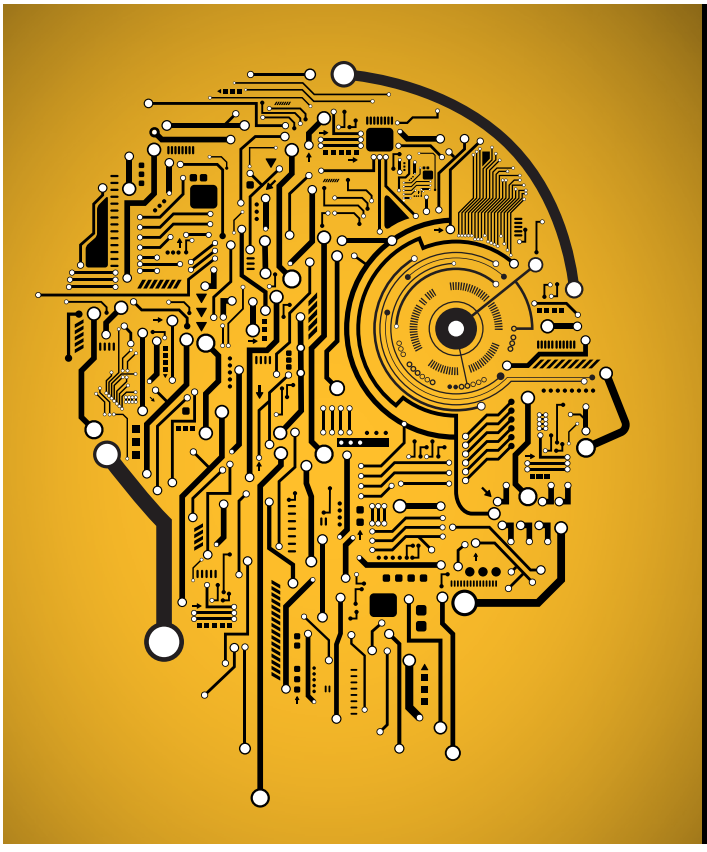


IN DEEP: The Art and Science of DFM with Gary Ferrari

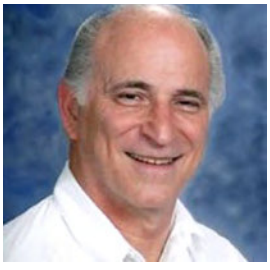
by Andy Shaughnessy
I-CONNECT007

When the topic of DFM techniques came up, I knew I had to talk with Gary Ferrari of FTG Corp. Gary has been involved with designing and manufacturing PCBs for decades, and he's the past co-founder and executive director of the IPC Designers Council. I caught up with Gary between Thanksgiving and Christmas, and we conducted the following interview via email.

***Andy Shaughnessy:** Give us a quick background on yourself and your role at FTG.*

Gary Ferrari: I have been in this industry for more than 50 years. The major portion of this time has been spent in PCB design and manufacturing. I have spent some time in assembly, industrial robotics, and nuclear and fossil power plant controls systems design.

I serve as the Director – Technical Support for FTG Circuits. My main function has many facets. First is to work with our customer base during the design phase of their products. I help them design for manufacture, which includes fabrication, assembly, repair, reliability, and field service. This includes end-product performance, both electrically and mechanically. It sounds like a lot, and it is. To meet today's advanced products within short design cycles, one must consider all these areas when selecting materials, components, etc.

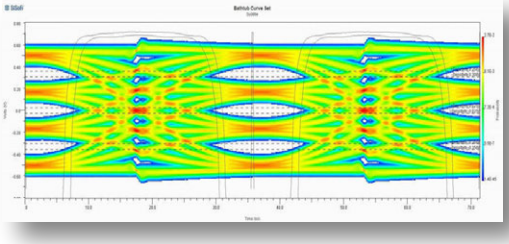


Gary Ferrari

Second is to represent them within the standards develop committees of IPC. Many current-day issues are discussed during the development meetings, which affect both our company and our industry. There are so many new, advanced technologies cropping up constantly. One must stay on top of them if one expects to survive in this industry.

I also provide IPC designer certification through EPTAC, an IPC licensed training center. These courses are quite extensive, exposing the attendees to many of the issues affecting successful designs.

We've been accelerating the design cycle for over 20 years.



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Shaughnessy: *So, what can PCB designers do to make the fabrication process go smoother?*

Ferrari: The most important item that a designer can do is to talk to their fabrication and assembly suppliers. Ask them about how your design practices are affecting their ability to manufacture with low yields and high reliability. Most important is to find out the areas that are the most troublesome. The designer has many ways to attack a given issue, and may be able to select a design solution that is easier to manufacture, resulting in higher reliability and lower cost. This is most important when doing a new design utilizing a technology that is new to the company. Most fabricators can draw from experiences gained through a wide variety of technologies they have worked with through a large customer base.

This also holds true about your assemblers. What are their capabilities and what are the costs associated with different technologies? What rules should the design follow in order to reduce cost and/or improve reliability? Are there panel, or component size limitations? Don't forget their testing capabilities and any specific limitations that should be reflected in the design.

In other words, there is much to be gained by communicating with your suppliers.

Obtain your fabricator's error rule files (ERF). This will enable you to check them against your rules to make sure that you are both on the same page.

Use industry standards when available. They are there to guide you as to how far you can push a design before negatively affecting fabrication, assembly, test, field service, and most important reliability.

Shaughnessy: *On the other hand, what are the most common mistakes that designers make that can slow things down during fabrication? I've heard of some CAM departments that stay busy with design data errors, especially from new customers.*

Ferrari: This is one area that really gets me going. I have spoken with customers that want to renegotiate a contract and cut costs by 30%. I tell them that we can do that by manufacturing the product on a larger panel with more boards produced per panel, resulting in a lower per-board cost. Unfortunately, we cannot do this with the existing board design, since the annular rings do not allow sufficient process allowances for registration, etch factors, material movement, etc. In many cases we are fighting for only a 0.001" additional annular ring.

What is frustrating is that the fix is free! All the designer needed to do was increase his padstack annular ring by 0.001" or more. Once the pad stack has been approved and placed into the system library, every time the padstack is used it will automatically meet fabrication requirements for a larger fabrication panel size. The designer will never notice that the lands are larger and will, in most cases, complete a design without being affected by the increase.

Insufficient annular ring is the number one hit that fabricators see. They spend a lot of time attempting to salvage a design by manually increasing annular rings, and moving adjacent conductors to maintain a minimum spacing requirement. Depending on the density and size of the board, this could be a monumental and costly operation.

Another big issue is that the designers are often not given the time to review their designs and run them through a DFM checker for spacing errors, annular ring violations, copper balance within and between layers, etc. Yes, some CAD systems have automatic design rule checking capability. But when having to move larger wired areas around of facilitate new changes, they tend to turn off the automatic DRC checking.

I tell designers to run their final output files through a third party DFM analysis prior to an official release. This will eliminate issues when sent out for final production. Most fabrication facilities will run a DFM analysis, prior to design release to you for little or no charge. Let's face it, when it is officially sent to the fabricator, the clock is ticking as it relates to time to market.

A second mistake that is common is not understanding all the aspects of a good layer stackup. Many of today's designs contain blind and buried vias. Thus, those layers with buried vias become plated layers that often increase the layer thickness, which in turn increases the overall board thickness. This can affect the ability to place the assembly into its final location.

Another problem related to blind and buried via stackups is determining the natural layer pairs. One must design a stackup from the inside out. In other words, you must start with the least common denominator…an inner layer, then build out from there, paying attention to the naturel layer pairs that need to be electrically connected.

Silk screen legends in component mounting holes, or on component lands. Legend inks are insulators and therefore will prevent an acceptable solder joint from forming.

Data errors have diminished over the years. But they still occur. One needs to reduce the number of different files needed to build a board, while providing more sophisticated data. The best way is to migrate to an intelligent data format such as ODB++ or IPC-2581. These formats support data extracted directly from your CAD database, and contain all information about the design, fabrication, assembly, test, etc.

Lastly, have a complete set of drawing notes and illustrations. Don't assume that your supplier knows what you want. State the exact material(s), line widths, spacing, non-conductive coatings, protective and metal finishes. Show a fully dimensioned board outline including and cutouts or special features.

***Shaughnessy:** Can a good (or bad) PCB design have a direct effect on downstream processes such as plating and surface finishes?*

Ferrari: Yes, the first is copper balance. It can affect the board in two distinct ways. The first is balance within a layer. Isolated conductors will etch faster than those conductors located in a dense copper area. This could result in less than minimum conductor widths in those areas. Remember, conductor width plays a huge roll in controlled impedance designs. Isolated traces will also plate faster, and heavier than those in a dense copper area. Excessive plating could bridge closely spaced lines in dense areas.

It is true that plating and etching equipment have gotten much better as these factors become less of an issue. But why tempt the hands of fate and leave that possibility open. Murphy's Law will almost guarantee that the issue will go against you. Throw in a properly grounded flood fill to negate the possibility of this issue occurring. The copper fill will help

balance the amount of copper on a given layer, thus reducing the possibility of an unacceptable level of bow and twist.

The second is an unbalance of copper from layer to layer. This could have a detrimental effect on overall board bow and twist.

The third is the use of multiple surface finishes. Downstream surface finishes could have an incompatibility with previously plated finishes. They may cross contaminate subsequent plating baths. The result is that the fabricator will have to utilize several masking and plating operations, which increase time and cost. I would recommend that if mixed surface finishes are necessary, that the designer consult with his fabricator on mixing surface finishes. This also holds true for use of mixed dielectrics.

***Shaughnessy:** What fab processes do you think designers should know more about? Most PCB designers tell me that they have never been to a board shop, or they haven't been to one for decades. Does that surprise you?*

Ferrari: I am not surprised that the majority of designers have never visited a board fabrication or assembly facility. The board designer has never been given their duly earned respect. They must fully understand the fabrication and assembly processes and their limitations, testing in both areas, laminate materials, protective coatings, repair and test strategies, component engineering, electrical characteristics and respective engineering, and new technologies. I could go on and on with what they should know. The sad part of it is that they are expected to know this purely by osmosis. Few companies actually allocate time for technical education. Few designers are allowed to go to major technology conferences, or attend standards development committee meetings. It is at these conferences that the learning opportunity is greatest. They also provide a perfect opportunity to develop a knowledge based support network.

There are quite a few designers that have joined IPC Designers Council chapters located throughout North America, Europe, Asia, and we must not forget the folks down under, in Australia. These chapters all run programs for designer education, plant tours, guest speakers, etc.

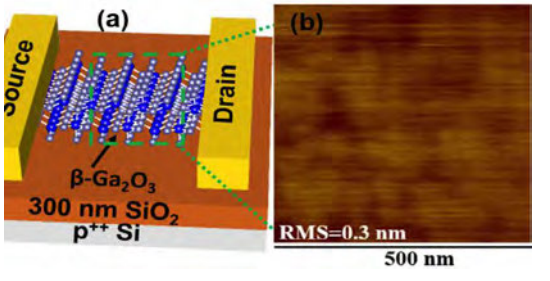
***Shaughnessy:** Is there anything else you would like to add?*

Ferrari: Those who know me know that I can go on forever. However, I think I have said enough. Thank you for the opportunity to vent.

***Shaughnessy:** Thank you, Gary.* **PCBDESIGN**

Semiconductor Eyed for Next-Generation 'Power Electronics'

Researchers have demonstrated the high-performance potential of an experimental transistor made of a semiconductor called beta gallium oxide, which could bring new ultra-efficient switches for applications such as the power grid, military ships and aircraft.



The semiconductor is promising for next-generation "power electronics," or devices needed to control the flow of electrical energy in circuits. Compared to other semiconductors thought to be promising for the transistors, devices made from beta gallium oxide have a higher "breakdown voltage," or the voltage at which the device fails, said Professor Peide Ye of Purdue University.

The team also developed a low-cost method using adhesive tape to peel off layers of the semiconductor from a single crystal. The "Scotch-tape" approach costs pennies and it can be used to cut films of the beta gallium oxide material into "nano-membranes," which can then be transferred to a conventional silicon disc and manufactured into devices, Ye said.

PCB007 Highlights

EuroTech: Institute of Circuit Technology Northern Seminar 2016, Harrogate

A new location for the Institute of Circuit Technology Northern Seminar: Harrogate, the elegant and historic spa town in North Yorkshire, England. And an impressive venue: the chandeliered drawing room of the palatial and stately Majestic Hotel, dating from the Victorian era.

Weiner's World

Here we go again! The winter holiday (and trade show) season is upon us. Electronica's mood was upbeat. Next, the Asia and San Diego shows. We just received word as we were preparing for our trip to next month's HKPCA/IPC event in Shenzhen, China that the CPCA show suddenly changed its March 2017 date and venue.

TTM President Thomas Edman on the Global PCB Market, Technology, and More

The TTM and Viasystems merger put the PCB industry on notice last year when it created one of the biggest powerhouses in the world. At this year's HKPCA and IPC show, Barry Matties met with TTM Technologies President and Chief Executive Officer, Thomas Edman to get his views on the market, technology, the culture of TTM and even the Trump effect.

KCE Group: A Thailand-Based PCB Manufacturer with a Growing Global Footprint

Recently, while at electronica in Munich, Germany I-Connect007's Judy Warner met KCE America President Rick Rhodes, and Joe Yeo of KCE Group. They discussed the unique challenges and opportunities that come with the rigorous automotive market, and explained why they continue to enjoy explosive growth.

EPTE Newsletter: Preliminary PCB Industry Results For 2016

I can't believe we are in the last month of 2016. We have almost a year of sales data from the global printed circuit industry, so this is a good time to analyze this year's performance and consider business plans for 2017. Since printed circuits are the major components in electronic products, let's review PCB market trends in the global electronics industry.

IPC APEX EXPO 2017 to Debut Flexible Hybrid Printed Electronics Pavilion

Apart from its more than 450 industry-leading exhibitors, the IPC APEX EXPO 2017 will debut its Flexible Hybrid Printed Electronics Pavilion to offer attendees a great opportunity to experience how these trending printed electronics products and technologies apply to hybrid PCBs and PCB assemblies.

All About Flex: Disruption in the Supply Chain

Manufacturers need a highly dependable supply chain to successfully support their products. This is especially true of custom designed and built components, as many times, only one supplier is available for a component since tooling and development costs discourage dual sourcing.

IPC: Connected Factory Initiative Subcommittee's Progress on Machine Data Interface Standard

Representatives of industry's leading manufacturers, machine, device, sensor and software companies that comprise IPC's 2-17 Connected Factory Initiative Subcommittee have made significant strides in developing a machine data interface standard, "Connected Factory Exchange or CFX."

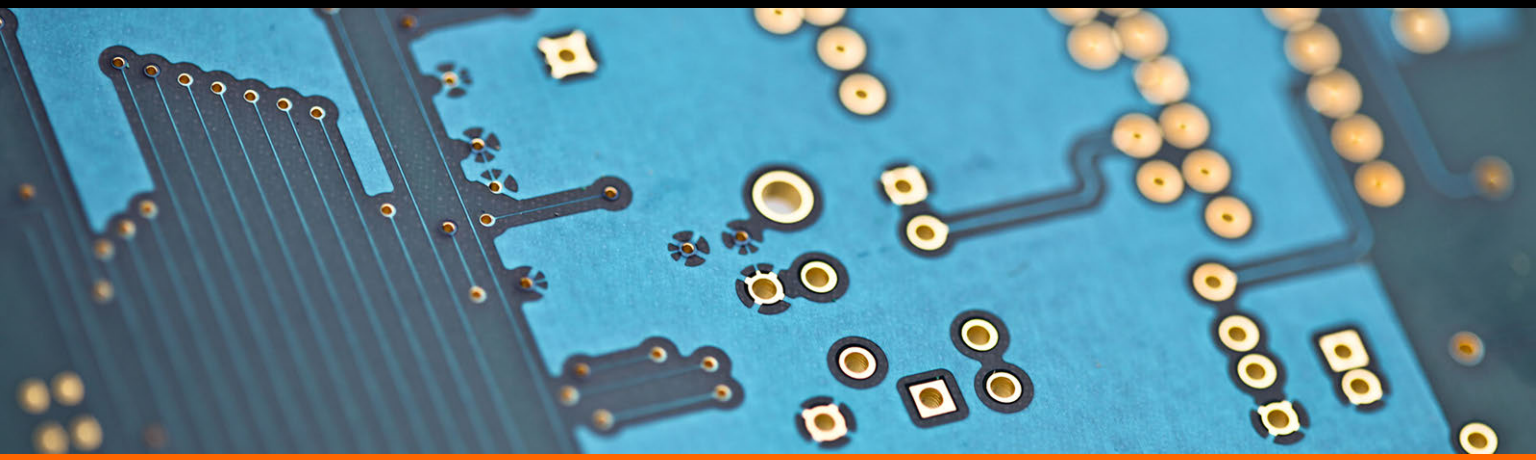
Innovative Use of Vias for Density Improvements

In today's fast-paced global, economic environment—which requires constant innovation, upskilling, and performance improvements— there is a need for increasing density. The classic way to increase density is to reduce the trace and spacing.

Launch Letters: Programs, Not Projects

Sometimes, an uncontrollable tick in my neck emerges. The wrinkle in my forehead that now has no boundaries slowly makes its way to my balding scalp. My porcelain china doll-like complexion gradually transforms itself to resemble a Honeycrisp, and ultimately, a Red Delicious apple.

SUNSTONE CIRCUITS *from Prototype to Production*



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PDN–Decoupling Capacitor Placement

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The impact of lower core voltages and faster edge rates has pushed the frequency content of typical digital signals into the gigahertz range. Consequently, the performance of decoupling capacitors, that are required to complement the power distribution network (PDN) and curb signal induced fluctuations, must also be extended up into this range. However, rudimentary design rules, adequate for frequencies below 100MHz, may not be suitable for today's high-speed digital circuits. The symptoms of an inadequate PDN design are increased power supply noise, crosstalk and electromagnetic radiation leading to poor performance and possibly intermittent operation.

In most cases, conventional design guidelines recommend that the decoupling (or bypass) capacitors be placed on the bottom side of the PCB, under the BGA, for closest proximity to the IC. However, decoupling is not the process of placing a few random capacitors adjacent to each IC power pin. But rather, it is the process of placing an RLC network to supply the transient switching current and to provide a return current signal path back to the source. A capacitor's equivalent circuit is basically a series capacitor, resistor and inductor as illustrated in Figure 1. These are referred to as the capacitance value, ESR and ESL respectively.

The primary design consideration is the

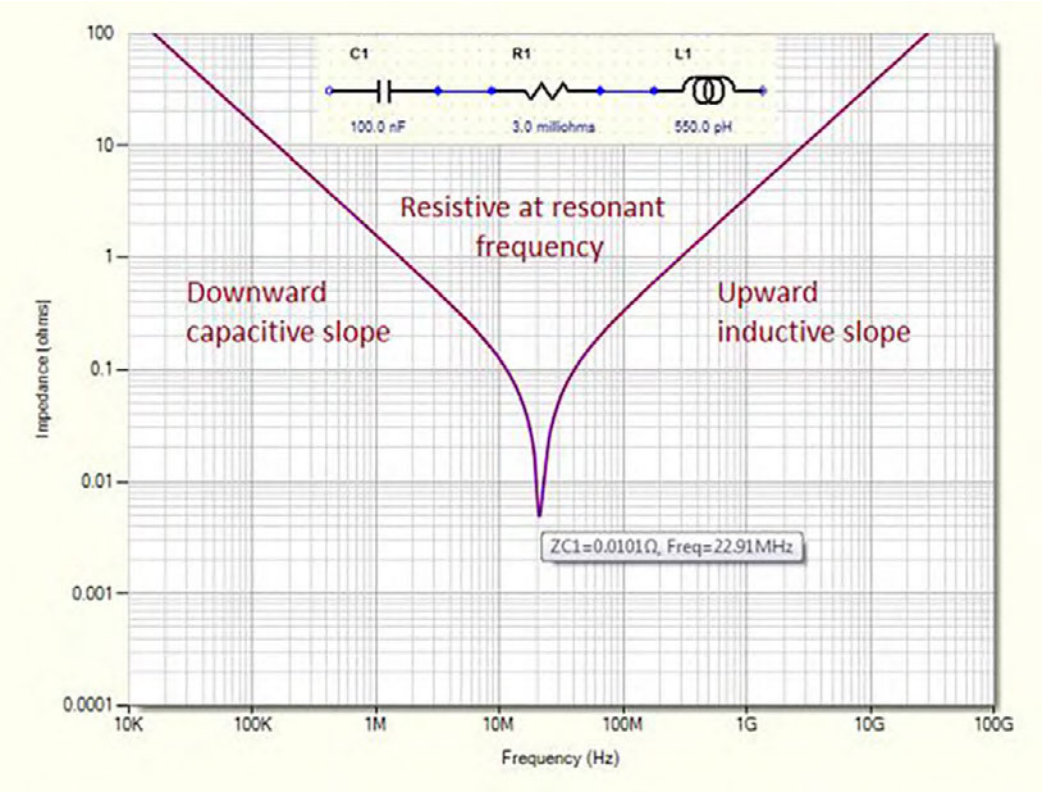

Figure 1: A capacitor has series capacitance, resistance and inductance.

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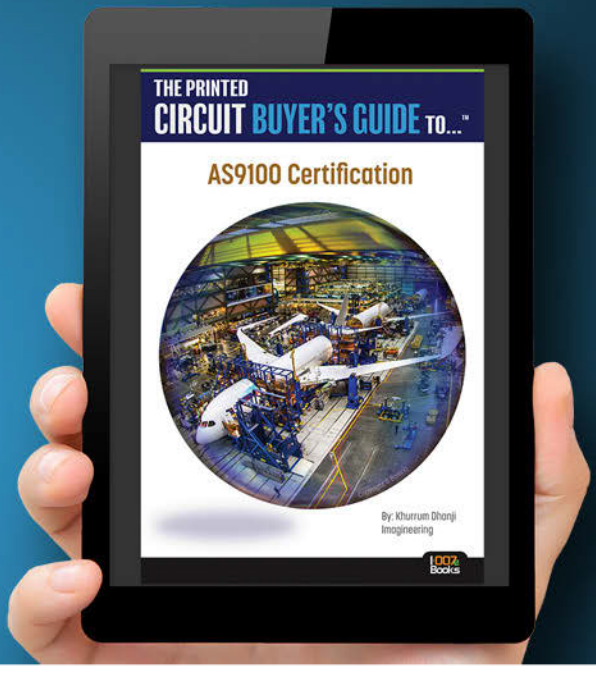

I-Connect007 is excited to announce the release of the first title in its *Printed Circuit Buyer's Guide to...* series, ***The Printed Circuit Buyer's Guide to... AS9100 Certification***.

Authored by industry veteran Khurrum Dhanji, of Imagineering, Inc., this is a must-read for buyers, specifiers, engineers or anyone involved in the procurement of printed circuit boards.

The *Printed Circuit Buyer's Guide to... AS9100 Certification* provides a high-level overview of the standard, as well as a breakdown of each of the five major requirements.

Look for these other exciting titles in our new micro eBook series to be released soon:

- ***The Printed Circuit Designer's Guide to... DFM*** by Altium
- ***The Printed Circuit Buyer's Guide to... Solderless Assemblies*** *by Joe Fjelstad*
- ***The Printed Circuit Buyer's Guide to... Flex Design*** by American Standard Circuits
- ***The EMS Buyer's Guide to... Procuring High Complexity Electronics*** by Zentech

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parasitic series inductance of the capacitor itself and its associated mounting and via inductance. The parasitic series inductance of a decoupling capacitor acts like a small inductor in series with the capacitor. At higher and higher frequencies, the impedance of this parasitic inductance becomes larger and larger (Figure 1), until it finally dominates the performance of the component.

In the critical 100MHz – 1GHz band, the effectiveness of a typical decoupling capacitor is determined almost entirely by its series inductance. This is the frequency band now being used increasingly by digital logic. For ideal performance, low series inductance is required. However, the series inductance of a capacitor is not only determined by its ESL, but rather almost entirely by the layout of the capacitor's mounting lands and its associated fanout vias. The exact location of the capacitor is unimportant (providing it is within a 2" radius of the IC) as the plane inductance is negligible. Every time the signal edge rates double, we become twice as dependent on these layout details. If a product radiates too much in this region, the most effective way to reduce noise is to improve the layout of the decoupling capacitor lands and to reduce the via loop area. Improving the layout reduces the effective inductance of the components, leading to a direct reduction in power and ground noise. It is the inductance of this current path that creates ground (supply) bounce. If the layout cannot be modified, then the following alternatives may suffice:

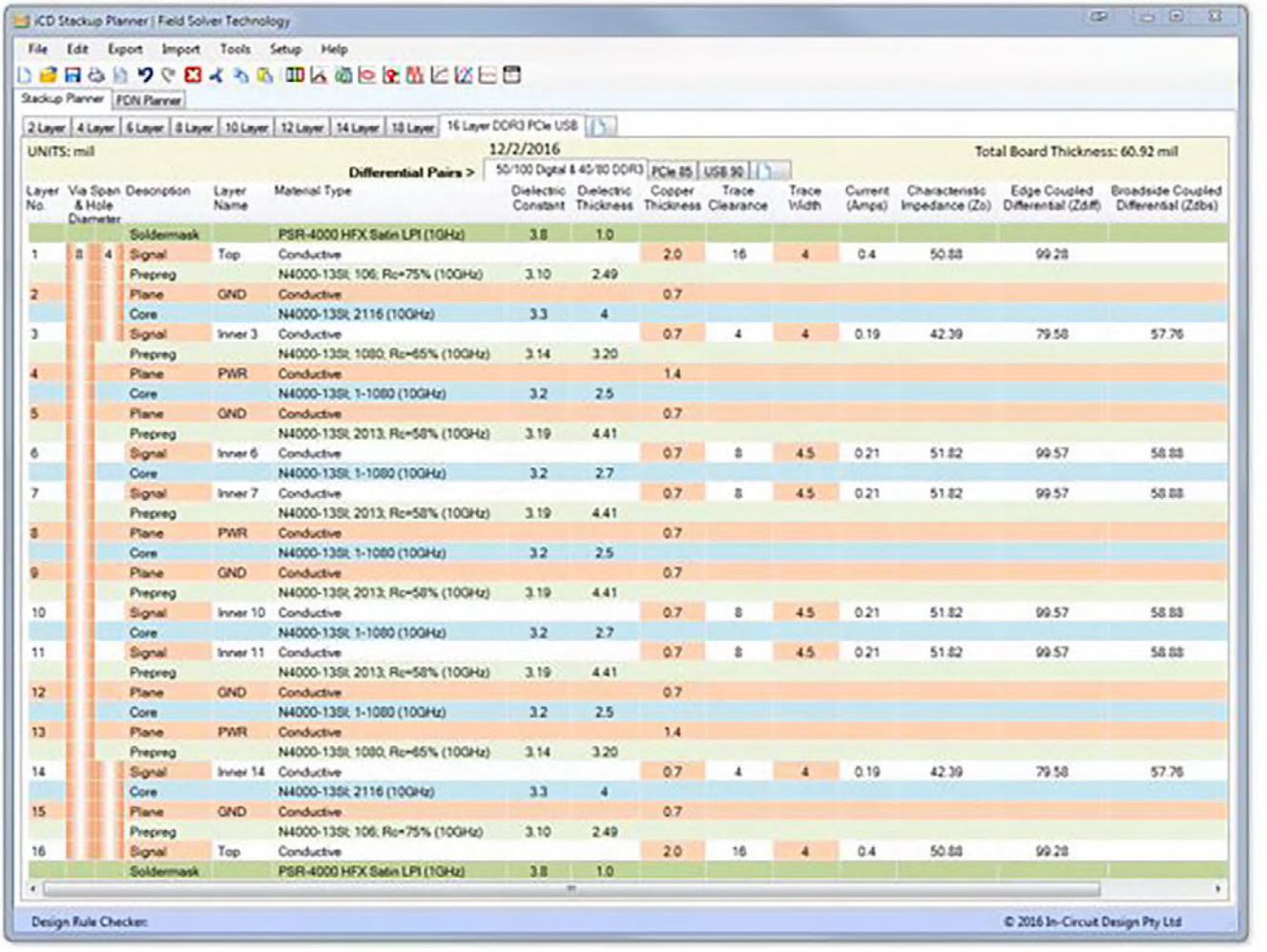

Figure 2: A 16-layer stackup with three pairs of planes.

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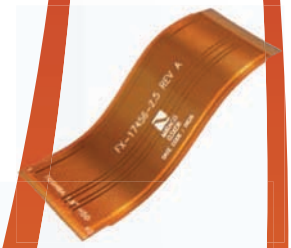

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1. Add more capacitors, but this will only add to the expense and consume more real estate.

2. Change the capacitor to a reverse geometry package with lower ESL – e.g. use a 0204 instead of a 0402.

3. Use a thin, high-dielectric constant (Dk) material between the planes, which adds more plane capacitance.

4. Use embedded planar capacitance material. This technology allows for a very thin dielectric layer (0.24 – 2.0 mil) that provides distributive decoupling capacitance and takes the place of many conventional discrete decoupling capacitors to some extent.

So, let's look at a typical 16-layer multilayer PCB with three plane pairs as in Figure 2. The total board thickness is 60.92 mils and the planes are symmetrically positioned in the stackup. Placing a BGA on the top side of the board and the decoupling capacitors directly under the BGA on the bottom side would require twice the total board thickness for the entire loop (power and GND vias) for each capacitor. In this case, the plane inductance can be ignored as it is insignificant. However, this is accounted for in the top mounting configuration by adding spreading inductance as the decaps cannot be placed directly under the BGA. The following calculations give the total loop distance for each configuration (Figure 3):

Amazingly enough, the bottom mount decap has about twice the current loop area as the top mount decap which equates to about twice the loop inductance. For example, a 22nF 0402 capacitor (Figures 4 and 5) has inductance of 1.28nH mounted on the top and 2.85nH on the bottom side. The most important specification for a decoupling capacitor is its series inductance and here we have more than doubled that inductance by following conventional design rules. These rules have been in use for over 25 years, so maybe it is time for an update!

Figure 4 illustrates the effective AC impedance of the bottom mount decoupling capacitors, including via loop inductance, of the 16-layer PCB extracted from the ICD Stackup Planner. To keep the impedance below the target impedance, all the way up to 1GHz, requires 82 optimized decaps. Please note that I have also used close coupling (2.5 mils) between the planes which dramatically improves the planar capacitance.

Figure 5 illustrates the effective AC impedance of the same decaps mounted on the top side of the board. Note how low the impedance is at the top end. Where the bottom mount decaps were below the target frequency up to 1GHz, the top-mount decaps are below to 2.5 times the fundamental frequency (2.5GHz). And, the capacitor count (Table 1) can be reduced from 82 (bottom mount) to just 38 (top

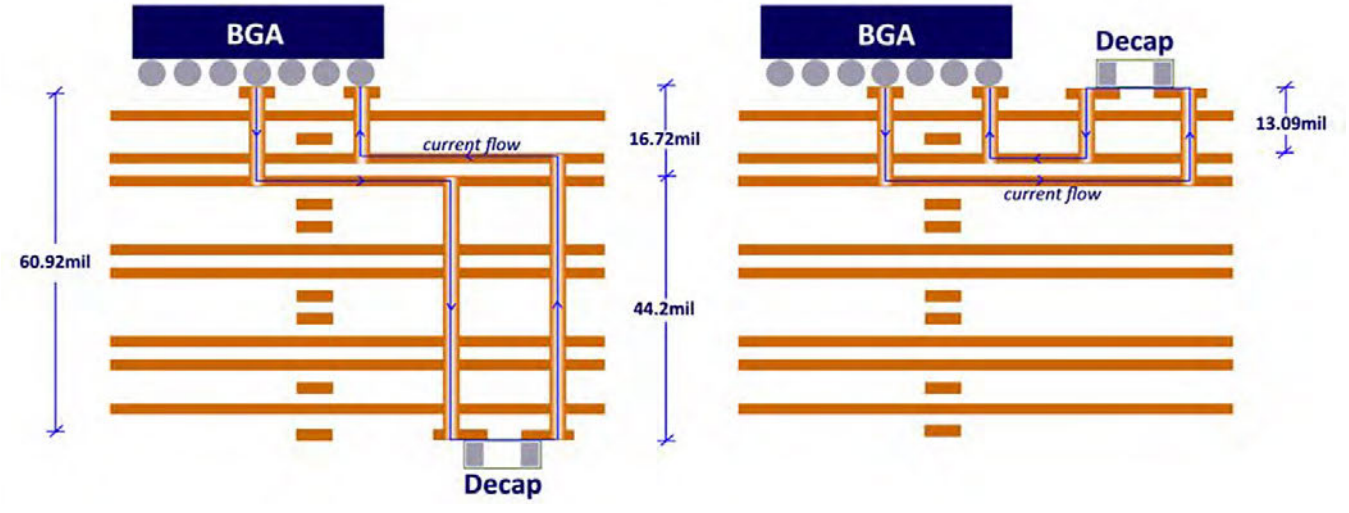

Figure 3: Decoupling capacitors placed on bottom vs. top of board.

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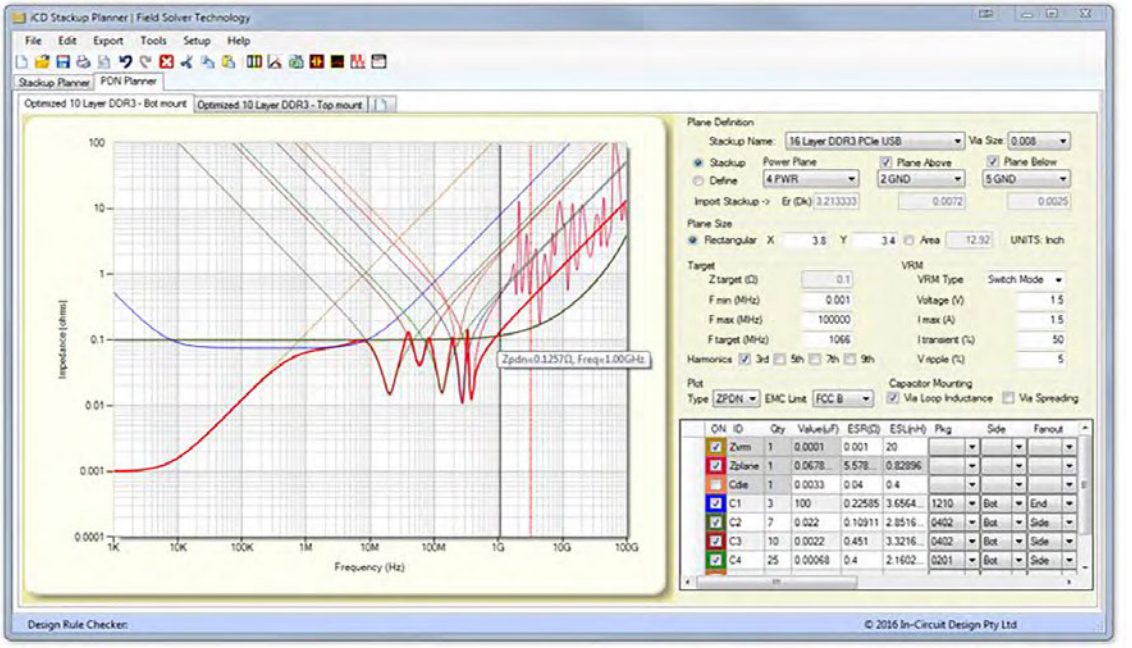

Figure 4: PDN analysis of the bottom mount decoupling capacitors.

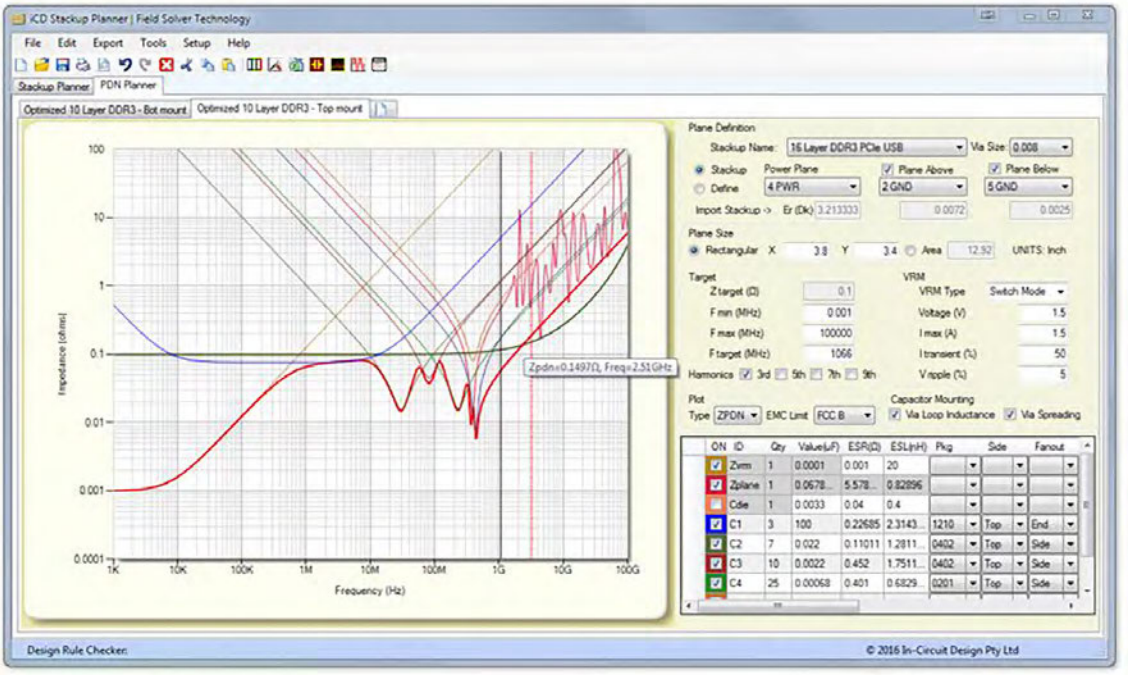

Figure 5: PDN analysis of the top mount decoupling capacitors.

mount) with greater bandwidth at half the cost and assembly time and superior performance.

This potential gain depends on the layer count and how the planes are arranged in the stackup. If the planes are central, as in a typical six-layer configuration, then the top- and bottom-mount inductance will be the same. But for a high layer count stackup, planes are best positioned close to the IC, with the decaps mounted on the same side, to reduce inductance. It is this configuration that can benefit most from same side placement.

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Capacitor	Qty	Value (uF)	ESR (Ω)	ESL (nH)	Pkg	Side	Fanout	SRF (MHz)	Dielectric	Type	Voltage	Tol %	Land	Part Number
C1	3	100	0.22585	3.656467	1210	Bot	End	0.375		TANT	6.3	20	1210	T494B107M006AT
C2	7	0.022	0.10911	2.851676	0402	Bot	Side	38.44	X7R	CER	16	10	0402	C0402C223K4RAC
C3	10	0.0022	0.451	3.321676	0402	Bot	Side	96.023	X7R	CER	50	10	0402	C0402C222K5RAC
C4	25	0.00068	0.4	2.160288	0201	Bot	Side	405	X7R	CER	16	10	0201	GRM033R71C332KA88
C5	7	0.00022	0.5566	2.233288	0201	Bot	Side	620	X5R	CER	25	10	0201	C0603X5R1E221K030BA
C6	30	0.00015	0.194	2.414347	0805	Bot	Side	637.6	C0G	CER	50	10	0805	CL21C151JBA
Total	82													

Bottom mount decaps including mounting inductance

Capacitor	Qty	Value (uF)	ESR (Ω)	ESL (nH)	Pkg	Side	Fanout	SRF (MHz)	Dielectric	Type	Voltage	Tol %	Land	Part Number
C1	3	100	0.22685	2.31436	1210	Top	End	0.375		TANT	6.3	20	1210	T494B107M006AT
C2	7	0.022	0.11011	1.281118	0402	Top	Side	38.44	X7R	CER	16	10	0402	C0402C223K4RAC
C3	3	0.0022	0.452	1.751118	0402	Top	Side	96.023	X7R	CER	50	10	0402	C0402C222K5RAC
C4	25	0.00068	0.401	0.682923	0201	Top	Side	405	X7R	CER	16	10	0201	GRM033R71C332KA88
Total	38													

Top mount decaps including mounting & spreading inductance

Table 1: Bill of materials for bottom-mount decap vs. top mount.

If your designs are working well today and decoupling is not a problem, don't be complacent. Progressive advances in the speed of digital logic will cause problems soon enough. Continual adjustment of decoupling capacitor value, package, mounting and routing rules is the only safe course of action. It is the inductance that limits the effectiveness of the PDN. It is very important to remember this fact.

Points to Remember:

- Rudimentary design rules, adequate for frequencies below 100MHz, may not be suitable for today's high-speed digital circuits.
- These design guidelines recommend that the decoupling (or bypass) capacitors be placed on the bottom side of the PCB, under the BGA.
- Decoupling is the process of placing an RLC network to supply the transient switching current and to provide a return current signal path back to the source.
- In the critical 100MHz—1GHz band, the effectiveness of a typical decoupling capacitor is determined almost entirely by its series inductance.
- The series inductance of a capacitor is not only determined by its ESL, but almost entirely by the layout of the capacitor's mounting lands and its associated fanout vias.
- The most effective way to reduce noise is to improve the layout of the decoupling capacitor lands and to reduce via loop area.
- In this case, the bottom mount decap has twice the loop area, for current flow, as the top mount decap which equates to about twice the loop inductance.
- Same side placement, reduces the capacitor count from 82 (bottom mount) to just 38 (top mount), in this case, with greater bandwidth at half the cost and assembly time and superior performance.
- For a high layer-count stackup, planes are best positioned close to the IC, with the decaps mounted on the same side, to reduce inductance. **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: PDN Planning and Capacitor Selection, Plane Crazy, Material Selection for SERDES Design

2. Henry Ott: Electromagnetic Compatibility Engineering

3. Howard Johnson: High-Speed Digital Design

4. All screenshots taken from the iCD Stackup and PDN Planner software

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD) Australia. The company is a PCB design service bureau that specializes in board-level simulation. ICD has developed the ICD Stackup Planner and ICD PDN Planner software, which is available here. To contact Barry, click here.

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On December 1, 2016, Cartel Electronics Inc. and its affiliates signed a definitive agreement to acquire Cirtech Inc.

One World, One Industry: Strengthening Your Value Proposition to Boost Organization Success

John Mitchell's new column's title says it all: One World, One Industry. In the coming columns, the IPC president will be covering issues affecting the entire global electronics industry supply chain with specific expertise on global standards, education, advocacy and solutions.

Tin Whisker Mitigation Methodologies: Report from SMART Group, Part 1

Since the introduction of the RoHS legislation in 2006, the threat of tin-whisker-related short circuit failure from pure tin finished components has remained a major concern within the high-reliability electronics manufacturing industry. In this article, Editor Pete Starkey reviews a recent seminar by the SMART Group to discuss tin whisker mitigation methodologies and strategies.

IPC Study on N.A. PCB Industry Reports Growth in Milaero Market

Printed circuit boards for military and aerospace applications remain the largest vertical market segment for PCB manufacturers in North America, representing about one-third of the market. And it is the only vertical market segment expected to grow in 2016 as a share of the North American market, according to IPC's 2016 Analysis and Forecast for the North American PCB Industry.

Eltek Signs Definitive Agreement for the Sale of Kubatronik

Eltek Ltd. announced today that it has signed a definitive agreement for the sale of all the Kubatronik-Leiterplatten GmbH (Kubatronik) shares it holds to Mr. Alois Kubat, Kubatronik's only other shareholder and founder. The parties expect to consummate the transaction by the end of 2016.

Orbit International's Electronics Group Lands $1.23M U.S. Navy Contract

Orbit International Corp.'s Electronics Group has received an award from a U.S. Government Procurement Agency valued in excess of $1,230,000 for its MK 119 Gun Computer System Cabinet (GCSC).

Sanmina's Salt Lake City Facility Earns AS9100C Certification

Sanmina Corp.'s Salt Lake City, Utah facility has been awarded the AS9100C certification for printed circuit board assemblies (PCBAs), subassemblies and systems.

Ellsworth Now Authorized Distributor of Henkel Products for Aerospace Industry

Ellsworth Adhesives has announced that it is now an authorized distributor of Henkel's surface treatments and structural adhesive products for the aerospace industry in Canada.

Laser-based Navigation Sensor Could Be Standard for Planetary Landing Missions

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THE EVOLUTION OF PCB DESIGN AND DESIGNERS

by Barry Matties
I-CONNECT007

According to Rainer Asfalg of Altium, VP Sales EMEA, EDA companies owe it to their customers to provide much more than just a standard design tool. I met with Rainer at the recent electronica show to discuss the continued evolution of the design process towards automation, and what this might mean for the education and overall requirements of PCB designers going forward.

Barry Matties: *Rainer, in our pre-interview discussion, you gave us a little bit of your background and it sounds comprehensive. You bring a lot of insight from multiple disciplines and product types, which gives you a good, diverse foundation to draw from.*

Rainer Asfalg: Yes, I think this is important for understanding the markets and understanding customers. It puts me in a position to make the right judgment on what our customers are really asking for and what challenges they face.

Matties: *You're also a printed circuit board designer. You have hands-on practical experience. How many years did you design for before you started working for the factories?*

Asfalg: Five years. I worked at a service bureau, mainly doing classical digital design, but I also got involved in analog and RF applications.

Matties: *That's a broad spectrum. Being in a design bureau gives you a great look at what's going on and a cross-section of current technology. One of the things that we hear about designers is that they don't have a deep understanding of the PCB manufacturing process. From the perspective of a designer, what do you think about that statement?*

Asfalg: It's correct. That's why an EDA company's responsibility is to put automation in place to ensure quality, while freeing up designers from time otherwise spent on preparing manufacturing data. On top of this, when we look at how the profession has evolved, what actually is a designer today?

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***Matties:** That's a great question. Can you answer that?*


Rainer Asfalg

Asfalg: These days we deal with a completely different type of designer. In the past we had electrical engineers who captured the design on a piece of paper or, further down the line, were responsible for schematic entry. Then they handed this over to a PCB design department or a service bureau. Those PCB designers are now my age or older. So these classic PCB departments have gradually faded away. The new designers are now responsible for much, much more. It is not simply about capturing the design, rather they are responsible for the test strategy, the PCB design, and the manufacturing as well.

When you look at a product's development cycle, these tasks are just 25 or 30% of the overall picture, beyond which they have to deal with purchasing, check whether the right components are available, and so on.

We need to help these engineers by providing greater automation and more intelligent tools which can, for example, ensure drawings comply to a company's standards. That's the reason why Altium is bringing tools to the market to supply this new landscape of designers. In Altium Designer 16.1 we released Draftsman. This feature addresses exactly the point you just mentioned. With Draftsman we have a template-driven manufacturing drawing environment. The person responsible for a company's design standards creates a template. Afterwards the designer just takes the PCB and drops it in, and you're done. Because all the intelligence regarding company standards is in the template, the designer doesn't have to deal with it.

***Matties:** How well does that work?*

Asfalg: Very well, and what's more, this additional functionality is given to our subscription customers at no extra cost. I think this is a key point, because other companies will sell options like this for $4,000–$8,000. That's one of the reasons why Altium is so successful, because people get a lot for their money when they are under subscription.

We see this again with ActiveRoute, included in our new Altium Designer 17 release. Charles Pfeil, a guru regarding autorouting technology, was heavily involved in this project. ActiveRoute is also part of the subscription and it's a revolution in PCB design. All EDA companies provide auto routing capabilities, but in many cases, and I'm sure you've heard this too, designers say, "I can't use this autorouter because it doesn't do the job." The question is, why?

***Matties:** That's the question I have. Why? It seems simple.*

Asfalg: It's very simple. If you have a really complex board, 32 layers with 6 power layers, you can use the autorouter without any problem. But it's different if you are working on a computer board or consumer electronics. With this board, you may have two signal layers, plus power and ground layers. The horizontal/vertical structures don't work because you've got high pin-count devices and signal paths you have to follow. Using an autorouter with this approach doesn't get these designs routed and it doesn't work. The designer has to think up front regarding the design structure: placement, traces, signal paths, then how to arrange this with just two signal layers. These structures are always far away from horizontal/vertical ones.

Now the challenge is, how can we automate this but still give the designers full control? This is exactly what ActiveRoute does. It has fully automated capabilities. The designer can take a bundle of 100 guides and say, "Start here and then I think it goes here, and here, and here. Now route." And ActiveRoute completes the task. It gives the designer full control, while taking care of anything that can be done automatically, so it's also fast.

***Matties:** Does the skillset or education of a designer tend now to become less of a requirement because of the automation?*

Asfalg: I think we are moving more into this direction where PCB design is not the final phase of the design, but part of the development process. Designers today, right from the beginning when they have their first idea, are making refinements to their project throughout the entire design process. In empowering these refinements, it is Altium's responsibility to allow enough space to think, to leave room for the design to take form and evolve. To set up an autorouter, in the past you had to write scripts and handle command codes. We can take this away and give more room for innovative thinking.

Matties: ***That's where the experience comes into play. Anybody can operate the tool, it's that simple, but there's no substitute for real-world experience.***

Asfalg: Exactly. It's required.

Matties: ***Do you envision a day when you just say, "I want a board that does this, this, and this," and you press a button and it gives you some questions regarding the specs, like a wizard, and then it spits it out? It seems like you're not very far off from that.***

Asfalg: There are still some obstacles for this.

Matties: ***What do you think is the greatest obstacle?***

Asfalg: The biggest obstacle, and it's true for all EDA companies, is what we do today is more or less documenting what we already know. A really huge step would be to say, "Here's my idea and this is how it should work," then gradually add more IP as it becomes more detailed, coming step-by-step down to the level that I can eventually define protocols for my design. The protocol implies certain components, so this could be embedded in the tools. Then it comes down to the point that I have to look for a real component. Is this component in my company library, or do I have to look outside? All this information is there, but then the aspect of mechanical constraints comes into the game because now we get form factors and other constraints like cost, weight, and reliability.

So yes, there is an idea of how this could happen, but it's still a pretty tough job to get there.

Matties: ***I think it is as well, but it seems like software development is advancing at such a rapid pace currently. Do you see that rapid pace combined with the aging population of designers and the lack of youth in design as an issue as well? Who are going to be our designers of the future? Where do they come from? Are there school processes?***

Asfalg: At least in Europe, universities have increasingly-popular electronics and electronic design programs. Over the years it's always been a little bit up or down, but right now I don't see any drop-off. One of the challenges we have is to develop EDA software for these designers or young professionals who come through university without necessarily being computer geeks. They're used to tools like a smartphone: simple, easy to use, powerful and productive. I think it's a key challenge for us to respond to this need.

Matties: ***That's a very wise statement right there.***

Asfalg: If we would like to penetrate the market and sell our tools, we better adjust to the market needs.

Matties: ***I think the interface of the software itself makes a big difference to bring and attract people in. Now it's working with software as opposed to having to write code, so to speak, and that's a big difference.***

Asfalg: Making the tools easier to use, easier to deploy and easier to handle is a real challenge, because at the same time we have to balance that with adding more and more functionality to address different needs. It's not enough just to have a core PCB design tool. In the past year we released our PDN Analyzer because when we asked our user community, "What are the most pressing issues when you design PCBs?" they

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didn't say, "High-speed design," they came back and said, "Power distribution is really an issue." So that's one of the things we co-developed with CST. We used the technology from CST and have embedded this tool very closely into our flow, while keeping it easy to use.

Normally when you talk about power integrity it's a specialist tool and a specialist environment. The challenge here was to make it suitable for every PCB designer. That's why the PDN analyzer is easy to use and therefore able to address these additional needs.

***Matties:** We're here in your hometown, Munich. What's the mood of this market right now?*

Asfalg: The market is very healthy, which is one of the reasons why we recently opened a brand new office in Munich. When we look at the roots of Altium Europe, we started in Karlsruhe, Germany, which is one hour away from Frankfurt airport and three-and-a-half hours away from Munich. We were growing so fast we had to get new folks on board and expand our horizons. The decision was that the next office we opened should be in a place which is easily accessible, close to high-tech companies, and also put us in a position to reach out easily to all of Europe.

That's the reason why we chose Munich. It doesn't mean we've closed down Karlsruhe and moved to Munich. That's not the case. This is just an addition, but now we have an office which is easily accessible, close to our customers, and as you can see here at this trade show, there's an international community.

***Matties:** Just a couple of final questions. What advice would you give a young PCB designer?*

Asfalg: Stay tuned and stay current – because we're in such a fast-moving environment. Not just for Altium; I think it's true for everyone. People who get stuck in their comfort zone will be left behind by the industry. These days it is really important to stay on top of the latest technology, have a wide perspective, and know what's going on and what the trends are. Also for software, be aware of the latest developments because they will make your life easier. Deploy the most recent releases and keep up to speed with what's being developed.

That's also something I highly appreciate over here in Europe: there are a lot of companies who are genuine innovators and technology drivers. To become one of these they need engineers who are clued into what the future is and what's being developed. I think they should just utilize and use all these exciting things, because it is extremely exciting. The markets are moving away from vertical specialists, so having a wider perspective is much, much better.

***Matties:** Yes, a lot more opportunity. What's the greatest challenge of selling software? It seems to me that if I'm loyal to one brand or I've been using one brand for many years and I'm very comfortable with that, I would think that must be hard to go and commit somebody to switch. What's your take on that?*

Asfalg: There are different aspects that are able to trigger a switch. One important aspect is cost. A PCB design tool shouldn't be terribly expensive. Development cost is an issue for many companies. The other side is functionality. Does the tool provide the necessary functionality I really need for my job? The best environment and the best tool are those which give me the best price-performance ratio for the money I invested. This is the criteria by which you should choose.

Then there's always this aspect of, "Oh my God, when I switch, what does it really mean?" I'll need to convert my libraries and my designs. Then I'll need to train my people and it will take time until they are properly productive. One of the most important things for us with Altium Designer is that it's easy to deploy. Part of this is to make all of these transition processes as easy as possible. We provide translation tools for all major EDA software, so it makes the mi-

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gration manageable, that's one part, but then our tools are easy to learn, simple to install, and this shortens the ramp-up phase.

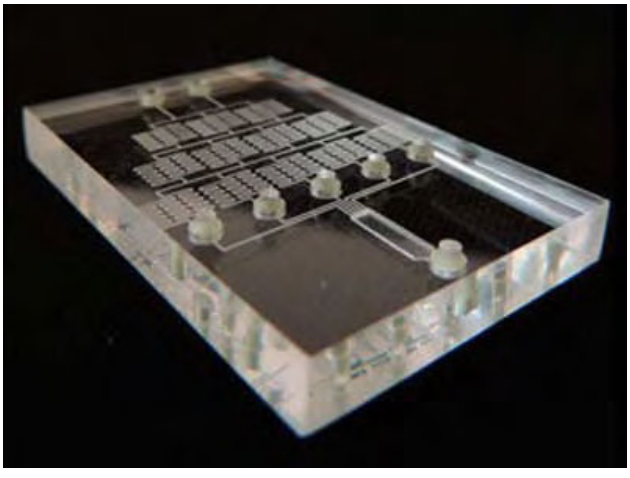
Then there's the training aspect, and this is one area we are expanding on right now, in order to offer different flavors of training. A designer could be trained in our facilities, another could be trained on-site, but then a lot of companies say, "I can't afford to have my team gone for one week for training. There are travel expenses, hotel costs, and they don't work on their projects. Make it easier for them to get trained!"

We need to offer both online training and on-demand training as well. All these aspects play into this philosophy of "easy to use, easy to deploy." I think it's our responsibility to lower the bar and make it simple to move across. There are a lot of people who want to move. People are highly interested in our design environment and what we provide. It is also our responsibility to enable them to do a realistic risk assessment of the transition and make the process as straightforward for them as possible.

***Matties:** Rainer, I certainly appreciate your time today. It's been great to sit down with an expert.*

Asfalg: It was great talking to you. **PCBDESIGN**

A Modular Valve Simplifies Diagnostic Chip Fabrication



Swapping delicate microscopic flow valves for a universal modular valve system has enabled A*STAR researchers to dramatically decrease the cost and complexity of microfluidic diagnostic chips—business card-sized devices that can analyse blood on the spot for a range of disease biomarkers.

"Microfluidic chips are advancing point-of-care diagnosis for many diseases," says Alicia Toh from A*STAR's Singapore Institute of Manufacturing Technology (SIMTech). "Inside these chips, tiny microvalves precisely direct microlitres of fluid through a series of microchannels for automated analysis. However, integrating microvalves into the microchannels is complex and highly susceptible to fabrication defects, which translates into a higher cost per device."

Toh and her colleagues Zhiping Wang and Zhenfeng Wang addressed the problem by moving the microvalves off the main microfluidic chip, and created a modular valve that is fitted to the surface of the chip after fabrication. The team demonstrated that their modular valves could precisely manipulate chemical concentrations through fluidic routing, which is critical in many advance diagnostic applications.

"By mass producing these microvalve modules separate from the microfluidic chip and testing valve function prior to chip integration, we can achieve much lower defect rates, which boosts yields and results in a much lower cost per device," says Toh. "This technology will reduce waste and help contribute to sustainable manufacturing practices for microfluidic chips."

Getting the valve design right, however, was complicated. The team used state-of-the-art software to predict the microscopic interactions between the flexible elastomeric silicone membrane and the fluid in the microchannel. Using materials that are compatible with the latest microfluidics technologies was also a big constraint.

Toh and her team are now exploring the production of microvalve modules using a variety of novel materials. "Greater adoption of microfluidic technology will mean that we could see our modular microvalves being used in a wide spectrum of applications," she says.

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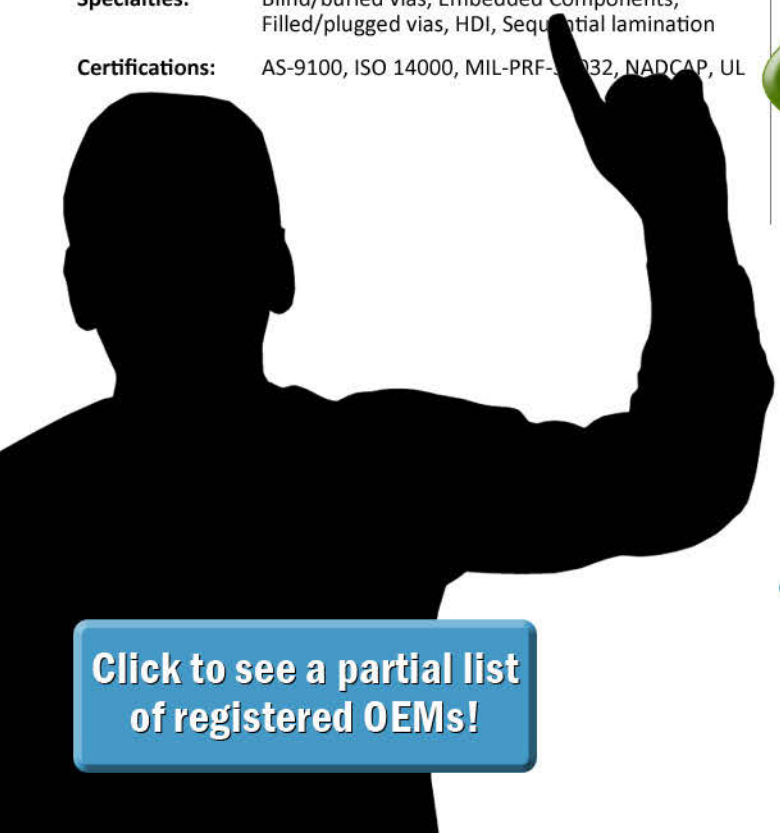
Certifications:	AS-9100, ISO 14000, MIL-PRF-3[illegible]32, NADCAP, UL



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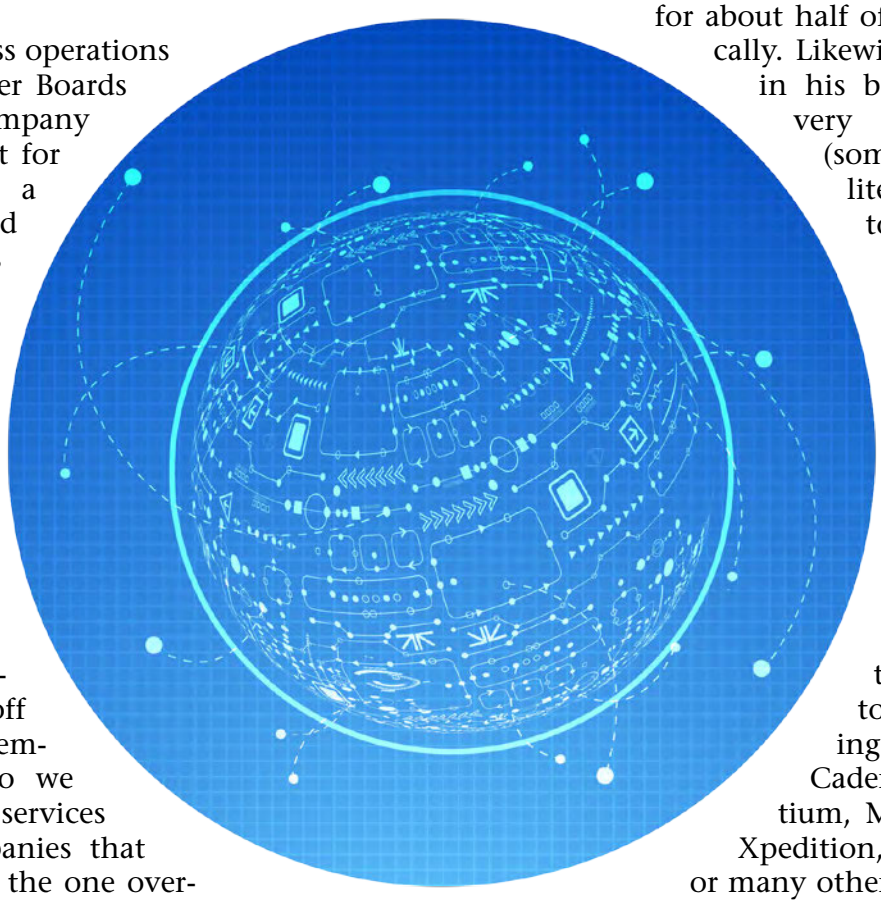
Selling PCB Design Services in a First-World Country

by Lance Olive
BETTER BOARDS INC.

Quality PCB design is an evolving breed of services in first world countries. As North American and European companies squeeze the skilled designers out of their own workforce, pushing more of the work into Eastern Europe and Asia, those who remain with the skills either opt for retirement, career change or consolidation.



As the business operations manager for Better Boards Inc., I see our company at the focal point for consolidation: a gathering of skilled board designers to create a center of excellence. It is at this point that we have the critical problem facing a PCB design services company: How do we effectively sell these services back to the companies that cast off their own skilled employees? How do we sell PCB design services into small companies that can barely afford the one overworked electrical engineer that they hired last year?

In addressing these key questions, we evaluate the three key challenges and embrace the three tantalizing opportunities. Doing this well gets our foot in the door and positions us to sell these services in the hardware design teams that would prefer to be designing circuits rather than layouts.

The Challenges

The first challenge is the price competition from both overseas labor and the designer working from home. PCB design layout service rates in Europe and North America remain relatively high for companies who know the value of the skill that designers bring. Meanwhile, small companies in the Czech Republic, Poland, India, Russia, Malaysia, the Philippines, Vietnam and China can offer layout services for about half of those domestically. Likewise, the designer in his bonus room has very low overhead (sometimes quite literally, thanks to knee walls), and can often undercut the hourly rates of a proper services company.

The second challenge is that of being multilingual in CAD tools. Between the customers demanding that we use Cadence Allegro, Altium, Mentor Graphics Xpedition, Eagle, KiCAD or many other cheap and free tools, it's enough to drive a designer mad. No person can reasonably support all of those. To support multiple customers means to support multiple tools. This is difficult to achieve with just one or two designers, since most professional designers are great at one tool, fair with another, and merely aware of the rest. Being successful means establishing a team of designers with varying skillsets—a matrix of

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Figure 1: Lance Olive, center, and the rest of the Better Boards staff.

designers with a mix of tool knowledge that can support any type of RFQ that comes in.

The third challenge is the commoditization of board layout. Tool vendors tout autorouting as their newest, most improved, wonderful feature. Electrical engineers prefer to hand off their schematics to someone else to "route the wires." After all, how hard can it be to connect the dots, quite literally?

The expectation is that the layout phase shouldn't be all that difficult, but we all know that as technology pushes us into hyper-fast clock signals and escaping 0.2 mm BGA pins in the smallest number of layers possible, it often does feel like a game of Jenga, Tetris and Candy Crush Saga, all rolled into one. The expectation oversimplification of the layout phase of design leaves many of us pulling out what's left of our hair.

But where there are challenges, there also lie opportunities, especially those that give us a competitive advantage to nullify the challenges.

The Opportunities

The first opportunity is that of a fast turn time. Even though no one plans to be in a hurry, many product development teams, especially their managers and PMs, take longer than expected to get the schematics underway. And when it's time for layout, they have very little time, want us to start tomorrow and be done in about half the estimated schedule. This is an opportunity for those who have developed an internal process that allows them to actually deliver. And when sitting in the office of a prospective customer and you can tell stories of delivering under duress, it makes the sales job so much easier.

The second opportunity is that of service. In many senses, this is the same axiom that you'll find in most businesses. In our line of work, if we can make the life of an engineer, a manager or a project manager easier by picking up their pieces, arranging an accurate, timely, best-practice-following board layout so they only need one spin before they are ready to make the push to production, we have provided a service to them that engenders happiness in their own job, creates a level of trust, and becomes their path of least resistance to product success. The loyalty that grows from this is very difficult to sever. Selling services where service is truly the core competency being delivered becomes easier.

The third opportunity is one of design accuracy. Getting the board right the first time means investing in reviews on the front end,

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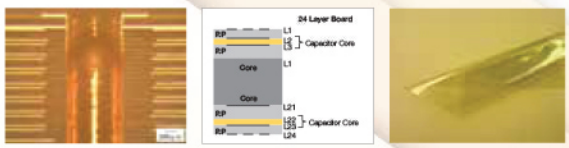

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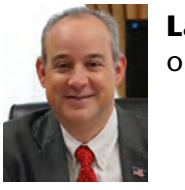
and saves time and money downstream. I come from the software industry, and we would employ a technique known as development phase containment. This concept involved selectively reviewing and approving the design along the way to contain the software bugs to the development phase closest to when they were created. Said another way, when a mistake is made, do what it takes to discover and fix it as quickly as you can because the cost of fixing it later can double every day that it goes undiscovered.

In the world of PCB design, this can take the form of a pin assignment problem, missing pull-up resistors, incorrect assumptions about amplifier behaviors, incorrect x/y/z dimensions for component placement, and reversed polarity, just to name a few examples. One the best comments I can make to a prospective customer is to let him know how many of our designs involve just a single iteration before heading to production (although product marketing can change the best-laid plans).

Summary

A company that can embrace these opportunities while meeting these challenges head-on by changing the way they do business creates fantastic sales stories that enable the sales representative to walk into any prospective customer situation – outsourced, tool-centric, fast-paced, floundering, tight-budgeted, endless iteration – and lay down a scenario that meets them where they are, engenders trust and opens the door to just a small enough crack that, once opened, will open again and again.

Selling PCB design services is only made easy when the company supplying those services has done all it can do to provide these stories and win prospective customers' hearts. **PCBDESIGN**



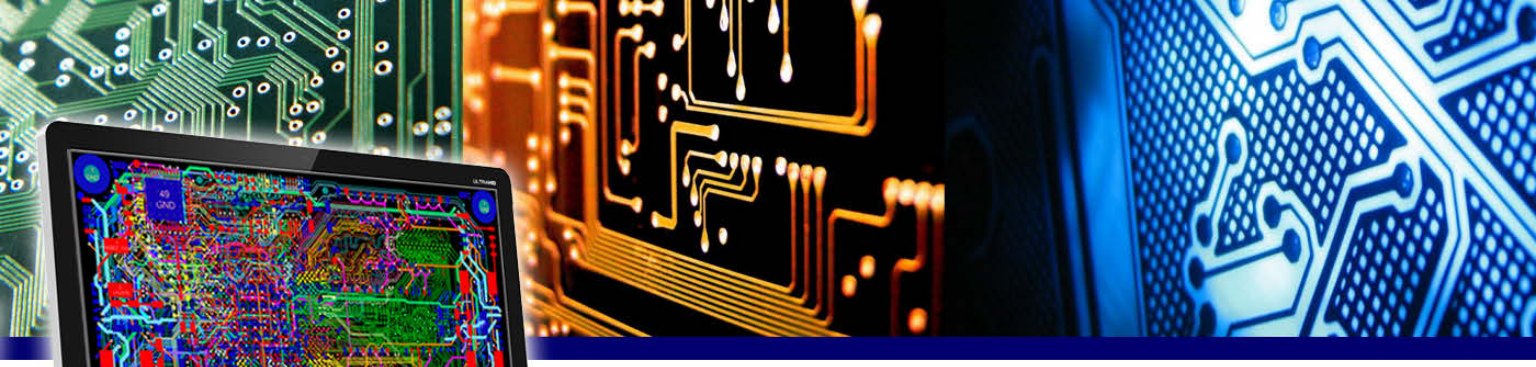
Lance Olive is director of business operations for Better Boards Inc.

Sharing Battlefield Info at Multiple Classification Levels via Handheld Devices

Troops in remote regions around the world often struggle to operate with limited networks for data sharing and communication. The usual process for sharing such information requires an end-to-end connection to secure servers via a dedicated digital "pipe" approved for the specific security level of data being transmitted. Additionally, the current computers and infrastructure needed to manage multiple levels of U.S. classified and coalition information are too bulky for tactical use in the field and can take months or longer to deploy.

To overcome this challenge, DARPA has announced its Secure Handhelds on Assured Resilient networks at the tactical Edge (SHARE) program. SHARE aims to create a system where information at multiple levels of security classification could be processed on a single handheld device using a resilient secure network that links devices without needing to route traffic through secure data centers. This capability would be able to operate over existing commercial and military networks while maintaining the security of sensitive information and safety of operations.

The end goal of the program is to demonstrate secure exchange of information at multiple levels of classification over unsecured military and commercial networks (e.g., Wi-Fi and cellular) using a heterogeneous mix of devices—from tactical radios to laptops to handheld devices.



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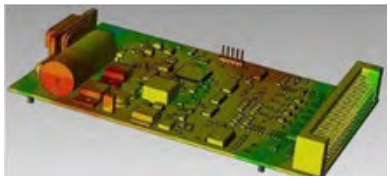
TOP TEN

Recent Highlights from PCBDesign007

1 EMA Releases Updated Power IC Model Library for PSpice

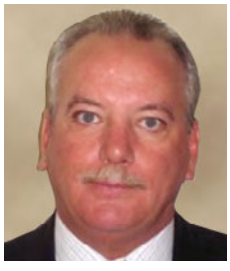
EMA Design Automation and AEi Systems, a world leader in power electronics modeling, analysis and design, has released version 4.2 of AEi Systems' Power IC Model Library for the Cadence PSpice simulator. "We've spent over 1,000 man-hours testing, simulating, and optimizing the new models in this release," said Charles Hymowitz, managing director at AEi Systems.

2 Mentor Graphics White Paper: Reduce PCB Failure Rates



Industry statistics indicate field failure rates of up to 15–20% in the first year for newly launched electronic products, resulting in warranty claims and high levels of field returns. In harsh environments, fatigue can be responsible for up to 20% of these product failures. This new Mentor Graphics white paper offers ways to reduce product failures.

3 Beyond Design: Uncommon Sense



When common sense fails, tap into your uncommon sense. Basically, common sense teaches us that the way it has always been done is the right way, and that's just how things are. Following common sense is usually the safe way to go. But the people who are really making a difference in the world are usually the people who try something new. Tapping into our uncommon sense allows us to take a look at things we often take for granted.

4 SiSoft Discusses Signal Integrity Drivers and Challenges

In the last few years, SiSoft has launched a variety of innovative SI tools that help automate tasks that used to take weeks or months to complete. I recently interviewed CEO Barry Katz via email, and he detailed their customers' challenges, and some of the market drivers in the world of signal integrity.

5 Top 10 Most-Read Design Articles of 2016

Every January, I like to go back through the last year and see which articles had the highest number of views. They're usually the articles that bring you PCB design and industry information that's relevant to your job. Check out the most-read PCB design articles from 2016.

6 Sales and Marketing with DownStream Technologies

From its inception, DownStream Technologies has been a new kind of software tool company. DownStream's post-processing tools address one of the most unpopular parts of the design process: documentation. DownStream's CEO Rick Almeida discusses some of his firm's marketing and sales methods, the trends that he sees, and the influence of the Internet on marketing.

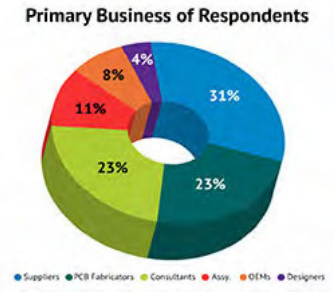
7 Ucamco Releases Integr8tor v2016.12

Ucamco has launched the v2016.12 maintenance release of Integr8tor. This release features important extensions and enhancements to existing functionality and addresses a number of software inconsistencies that were reported by our Integr8tor user base.

8 Sunstone Circuits Makes Shift in Strategy, Offerings

Sunstone has recently made a shift in capabilities that will enable a move into the RF and microwave space. At PCB West, I caught up with Sunstone's David Warren, and we discussed details of this change and how they plan to approach such a competitive marketplace.

9 Much Ado About Sales and Marketing



We at I-Connect007 recently surveyed our readers to get a better idea of what company leaders thought about sales and marketing. The results were informative, at times surprising, and even a bit disappointing, especially when some of the participants reported that they had no sales and marketing plan at all.

10 T-Tech Releases IsoPro 4.0

T-Tech Inc., the manufacturer of the Quick Circuit rapid prototyping system, has launched IsoPro 4.0. IsoPro 4.0 edits and converts Gerber, Excellon Drill, and DXF files for use by the Quick Circuit prototyping systems in order to fabricate circuit boards.

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Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

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January 18–20, 2017
Tokyo Big Sight, Japan

DesignCon 2017
January 31–February 2, 2016
Santa Clara, California, USA

EIPC Winter Conference
February 2–3, 2017
Salzburg, Austria

MD&M West
February 7–9, 2017
Anaheim, California, USA

IPC APEX EXPO 2017 Conference and Exhibition
February 14–15, 2017
San Diego, California, USA

China International PCB & Assembly Show (CPCA)
March 7–9, 2017
Shanghai, China

14th Electronic Circuits World Convention
April 25–27, 2017
Goyang City, South Korea

KPCA Show 2017
April 25–27, 2017
Goyang City, South Korea

IMPACT Washington D.C. 2017
May 2–3, 2017
Washington, D.C. USA

Thailand PCB Expo 2017
May 11–13, 2017
Bangkok, Thailand

JPCA Show 2017
June 7–9, 2017
Tokyo, Japan

IPC Reliability Forum: Emerging Technologies
June 27–28, 2017
Düsseldorf, Germany

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